Multiclass, Multistage, and Multilevel Fiber-Optic CDMA Signaling Techniques Based on Advanced Binary Optical Logic Gate Elements

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***Abstract*—In this paper we introduce and propose novel signaling methods and receiver structures based on advanced binary optical logic gates for fiber-optic code division multiple access (FO-CDMA) systems using all-optical signal processing. In the proposed system the users of the network are categorized into multiple classes. Users of each class transmit at the same power level but different from the levels of the other classes' users. Using a combination of optical OR, AND and XNOR logic gates for the receiver structure we show that such a network not only takes the full advantages of all-optical signal processing but also demonstrates a considerable throughput efficiency when compared to ordinary FO-CDMA systems. The proposed receiver structure mitigates the effect of interfering users from the other classes by rejecting some specified power level combinations from the other classes. The depth of interference cancellation is a function of the corresponding number of power levels and the number of stages applied to the optical logic gates in use. In our analysis we choose the generalized form of optical orthogonal codes (OOC), i.e., OOCs with cross-correlation value greater than one, as the signature sequence. We begin by emphasizing on two-level systems, that is, when the users can select one out of two power levels for signal transmission. However, for multilevel FO-CDMA we obtain a closed-form relation for the upper bound on the probability of error. We will show that under the ideal case the increase in throughput resulting from the proposed multilevel system is proportional to the number of classes or power levels in use. Our analytical results are compared to the results of an extensive system simulation. The numerical closeness between, the analytical and system simulation, indicates the accuracy with which we have modeled mathematically our proposed signaling using advanced binary optical logic gates in FO-CDMA.**

***Index Terms*—Fiber-optic CDMA (FO-CDMA), optical logic gates, optical orthogonal codes (OOC), multilevel signaling, optical and logic gate, optical XNOR logic gate, optical or logic gate, multiclass multistage OCDMA, multilevel OCDMA.**

I. Introduction

THE ULTIMATE quest for establishing all-optical processing in optical CDMA (OCDMA) systems and data networks will highly depend upon certain key enabling technologies and devices such as binary digital optical logic gate elements. Even though various physical phenomena have been introduced in implementing binary optical logic gate elements, at the fundamental device level all the proposed physical phenomena share a common input-output relation [1]. The most widely used physical phenomena in implementing optical logic gate elements is due to the input line intensity addition followed by a nonlinearity. As an example, Fig. 1 shows N-input lines where each line takes on the values of 0 or 1 (one-level signaling) and the intensities are summed to yield N+1 level signals, i.e., levels 0,1,..., or N. This signal is the input signal to the nonlinear device which produces a binary output, ideally a pulse with intensity zero for binary 0 and a pulse with intensity one for binary 1.

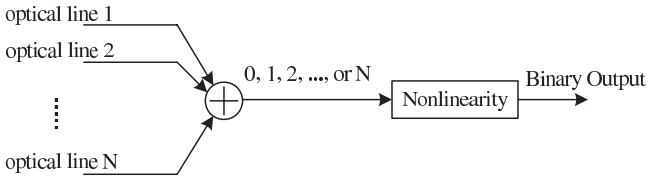

Fig. 1. Implementation of an N-input binary logic gate. Nonlinearities for implementation of N-input binary logic gate can include digital combinatorial logic operations such as OR, NOR, AND, NAND, XOR, XNOR

OCDMA systems based on optical orthogonal codes (OOCs), with length L and weight w, use one-level signals to establish its multiplexing and demultiplexing scheme [3]-[7]. Furthermore at the receiver front end of each typical OOC based OCDMA system with N users the intensity of the received signal due to the desired and multiple access interfering signals could be a N+1 level signal. This signal is the input signal to the nonlinear device which produces a binary output. Depending on the combinatorial logic function of the nonlinear device one can apply various logic operations such as AND, NAND, XOR, OR, NOR, and XNOR on this input signal. Interestingly, the nonlinear function consists ideally of thresholds placed at various input intensity values [1]-[2].

Taking advantages of various nonlinear functions one can devise various OCDMA systems, in particular, multilevel OOC based OCDMA system. Multilevel signaling corresponds to an OCDMA system in which various users' OOCs can take on different power levels. At the receiver end using OR, AND and XNOR logic functions one can distinguish OOCs with various optical power levels and remove those OOCs employing different power levels from the set of OOCs employing the same power level. In this paper we show that the throughput of networks using multilevel signaling are improved by a factor which is proportional to the number of the signal or power lev-

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els used in the system. As a matter of fact, recently, it has been shown in some research works that using multilevel signaling or having users with different power levels may improve the system performance if the transmitted powers are controlled and if the corresponding receivers have a complete knowledge on the power levels of the users [8]-[10]. For instance, in [8] a power control algorithm using variable optical attenuator prior to transmission has been proposed in order to maximize the capacity of a multirate fast frequency hopping OCDMA system. While in [9] authors have investigated a multirate OCDMA system with time hopping, a wisely-designed optical block, namely, optical power selector which consists of a set of optical hardlimiters and couplers has been inspected in this work for improving the system performance when the users transmit at different power levels. In [10] authors have proposed an OCDMA system with M-ary pulse amplitude modulation (PAM), applying the chip-level receiver with M-level threshold detection which is superior to OOK-CDMA systems in term of improving the bit error rate. Elsewhere multiweight orthogonal codes are also investigated to achieve differentiated QoS for an OCDMA network [11]. In [12] the authors present an algorithm for generating multiweight multilength strict OOCs to support OCDMA networks with arbitrary QoS and rate.

In this paper, we propose and study the use of binary optical logic gates including OR, AND and XNOR gates in order to design an all-optical receiver for a multilevel FO-CDMA system. Employing optical logic gates in FO-CDMA receiver not only gives us the advantage of ultra-fast optical signal processing but also mitigates the effect of multiple access interference (MAI) signal significantly as we show in the following sections. For our system description, we consider the ideal model for the optical gates and neglect the Poisson shot noise and receiver thermal noise in our analysis. We employ OOCs with cross-correlation coefficient, $\lambda \geq 1$, as the signature sequences. It has been shown that OOCs with λ = 2,3 not only presents a larger cardinality but also can improve system performance when compared to $\lambda = 1$ [7]. However, our performance analysis are obtained as a function of λ. Furthermore we present a throughput analysis in order to compare the performance of multilevel with that of an ordinary one-level FO-CDMA system. We show that the increase in the network's throughput is asymptotically proportional to the number of power levels used in the system.

Furthermore, we study the effect of multiple access interference (MAI) which is the dominant noise in any OCDMA systems. We obtain the floor limit of the system performance due to MAI and also obtain the maximum achievable number of users that are permitted to communicate simultaneously on the shared optical channel without exceeding a predefined BER. In general to obtain a thorough analysis for the power and the energy efficiency of the proposed system it is required to consider the main sources of noise such as shot noise, loss of fiber, loss of passive optical components, nonlinear effects of the fiber, noises due to optical gate elements employed in the proposed receiver structure. However, in this paper, we only consider MAI in order to highlight the essential features to our proposed signaling methods and receiver structures based on advanced optical logic gate elements.

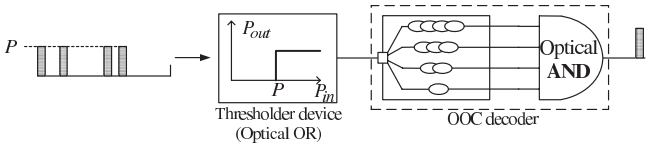

Fig. 2. OR and AND gate structure for FO-CDMA receiver

The rest of this paper is organized as follows: in section II we describe the model of a system which is based on optical OR and AND logic gate structures. We show that in this model if some users consume higher power level than the others, they achieve better performance without affecting lower power users' performance. In section III we introduce the receiver structure based on optical OR, AND and XNOR gates which improve the performance of both low and high power users simultaneously. Section IV generalizes the results of section III to a multilevel FO-CDMA system. Section V discusses and obtains the throughput of the proposed multilevel FO-CDMA system and compares its value with that of an ordinary one-level FO-CDMA system. Finally in section VI we conclude the paper.

II. Preliminary Discussions on Two-Level FO-CDMA System Model

The FO-CDMA system considered in this paper consists of N users communicating asynchronously through a passive $N \times N$ star coupler. To transmit its corresponding information bits each user employs an OOC stream as the signature sequence. We use the generalized form for the OOC set where the cross-correlation coefficient of the code sequence, i.e., λ, is an arbitrary value bounded by the code weight w. On the other hand, at the receiver end each user using its corresponding code structure decodes its information bits. We employ the well known AND logic gate receiver structure for the FO-CDMA receiver [7]. This structure is realized by a thresholder (OR logic gate) followed by a decoder that could consists of fiber tapped delay lines and an optical AND logic gate element as shown in Fig. 2. The thresholder's value, prior to optical decoder, is set at power level P which is the received optical power level of the desired pulsed chips that constitute the corresponding OOC code in use. For the sake of analytical simplicity we ignore the fiber loss and splitting effect of all optical passive devices within the network such as star coupler, encoder, decoder, and optical logic gates. In other words we assume that the transmitted pulsed chips at power level P are received at the same power level at the receiver side.

From Fig. 1, to establish an AND logic function the threshold Th is defined such that the input intensity I to the nonlinearity must satisfy the following condition: if $I \geq (Th = N)$ the output of the nonlinear device is one, otherwise it is zero. As another example to establish OR logic function the threshold Th is set at one, i.e., $Th = 1$, and if the input intensity $I \geq 1$, the output of the nonlinear function is one otherwise it is zero. The optical AND logic gate is modeled by a multi-input single-output device as shown in Fig. 3 [1]. If the sum of all input ports' power is greater than the value of the gate, the output generates an *on* or pulsed signal with a power level P_0, otherwise the output is *off*. One can check

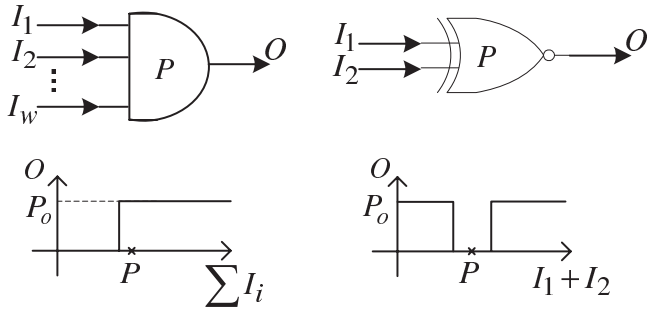

Fig. 3. Optical AND, XNOR gates' input/output diagram

that the thresholder device, i.e., OR logic gate, is equivalent to an optical AND logic gate with only one input port. The performance analysis of the system in Fig. 2, considering multiple-access interference (MAI) is evaluated in [7], also see Appendix A.

In many multiclass access networks one or more users intend to have a better quality of service, QoS, at the cost of higher power consumption or any other criteria that the system or network management indicates. Assume that for the above mentioned FO-CDMA network of Fig. 2, one out of the N users transmits at the power level of $P+\Delta P$ while the remaining $N-1$ other users transmit at the power level P. And also assume that the resolving power of the optical thresholder is within or better than ΔP [2]. In other words the optical thresholder device can distinguish between power levels P and $P+\Delta P$ with no ambiguity. The receiver threshold for each of the remaining $N-1$ low power users is set at P. Thus from the lower power user's receiver point of view, the interference caused by the higher power user, i.e., the user with power level $P+\Delta P$, on the marked pulsed chips of the desired lower power user is similar to the interference from other lower power users. Therefore the performance of low power users due to the presence of a high power user is not altered. On the other hand, the thresholder value of the high power user's receiver is set at $P+\Delta P$. In this case the interfering pulsed chips with power level P are eliminated at the output of the thresholder of the high power user's receiver. So, only, when at least two low power users hit on a marked chip of high power user, this chip is interfered. In a more generalized form if we have $cP<P+\Delta P\leq(c+1)P$, with c as a positive integer, a marked chip of the high power user is interfered if and only if at least $c+1$ low power users hit on a designated marked chip. The higher the value of the c the lower the probability of error for high power user, at the cost of more power consumption. Although the probability of error for low power users is independent of the number of high power users when the total number of users in the network is fixed, the performance of high power users degrades with increasing number of high power users.

Let N_1 be the number of class 1 users with lower power level, say P_1, and $N_2=N-N_1$ be the number of class 2 users with higher power level, say P_2. Let $cP_1<P_2\leq(c+1)P_1$, where c is a positive integer. Following the above discussion the probability of error for the class 1 users, P_{e1}, is a function of N which of course is obtained from eq. (A.5). However when we consider the desired user to be a member of class 2, i.e., high power users, the probability of error for a member of class 2 users, P_{e2}, depends either on N or N_2. If we denote by w the OOC code weight, for an AND gate receiver an error is occurred when all w marked chips of the desired OOC are interfered. The jth marked chip of a desired class 2 user is interfered by the class 2 interfering users if at least one class 2 interfering user hits the jth chip of the desired user. Furthermore the same jth marked chip of the desired class 2 user is interfered by the class 1 users if it is hit by at least $c+1$ class 1 users. In general the interference patterns that can cause an error can be categorized into $w+1$ disjoint groups. If so, the probability of error is obtained by the summation of the probabilities of occurrence of each group's events. The first group contains such patterns in which class 2 interfering users hit all w marked chips of the desired user's OOC code. The second group contains such patterns in which class 2 interfering users hit exactly $w-1$ marked chips of the desired user OOC and class 1 interfering users hit the single remaining marked chip. Continuing this procedure the ith group contains such patterns in which class 2 interfering users hit exactly $w-i+1$ marked chips and class 1 interfering users hit the remaining marked chips. Therefore if we denote the number of interferences on the jth marked chip of a class 2 user by α_j and considering the statistical independence among the users we can write:

$$P_{e2}=\frac{1}{2}\sum_{i=1}^{w}\binom{w}{i}\times\Pr\left(\alpha_1=0,\ldots,\alpha_i=0,\alpha_{i+1}>0,\ldots,\alpha_w>0\middle|N_2-1\ class2\ users\right)\times\Pr\left(\alpha_1>c,\ldots,\alpha_i>c\middle|N_1\ class1\ users\right)\quad(1)$$

To simplify the mathematical discussions on the above expression we define the following two functions f and g as follows,

$$f_i(N_2)=\Pr\left(\alpha_1=0,\ldots,\alpha_i=0,\alpha_{i+1}>0,\ldots,\alpha_w>0|N_2-1\ class2\ users\right)\quad(2)$$

$$g_i(N_1,c)=\Pr\left(\alpha_1>c,\ldots,\alpha_i>c|N_1\ class1\ users\right)\quad(3)$$

In Appendix B we show the following relation;

$$f_i(N_2)=\sum_{j=0}^{w-i}(-1)^j\binom{w-i}{j}\times\Pr\left(\alpha_1=0,...,\alpha_{i+j}=0|N_2-1\ class2\ users\right)\quad(4)$$

To obtain the right hand side of the above equation we can use eq. (A.3) where we have:

$$\Pr\left(\alpha_1=\ldots=\alpha_{i+j}=0\middle|N_2-1\ class2\ users\right)=\left[1+\sum_{l=1}^{\lambda}(-1)^l\binom{i+j}{l}\rho_l\right]^{N_2-1}\quad(5)$$

Where ρ_l is directly obtained from eq. (A.4): $\rho_l=\sum_{j=l}^{\lambda}\binom{w-l}{j-l}p_j$ and $\sum_{j=1}^{\lambda}j\binom{w}{j}p_j=\frac{w^2}{2L}$. L and w are the code length and the code weight respectively. p_j is the probability that one interfering user hits on just j specified chip pulse positions of the desired user's OOC. On the other

hand from Appendix B:

$$g_i(N_1,c)\leq \Pr\left(\alpha_1>0,\ldots,\alpha_{(c+1)i}>0|N_1\ interfering\ users\right) \quad (6)$$

We show in Appendix B also that:

$$g_i(N_1,c)\leq 1+\sum_{k=1}^{(c+1)i}(-1)^k\binom{(c+1)i}{k}\left[1+\sum_{l=1}^{\lambda}(-1)^l\binom{k}{l}\rho'_l\right]^{N_1} \quad (7)$$

Where we have $\rho'_l=\sum_{j=l}^{\lambda}\binom{w-l}{j-l}p'_j$ and $\sum_{j=1}^{\lambda}j\binom{(c+1)i}{j}p'_j=\frac{w(c+1)i}{2L}$. We have defined p'_j in Appendix B. Using (1)-(7) we have:

$$P_{e2}=\frac{1}{2}\sum_{i=0}^{w}\binom{w}{i}f_i(N_2)g_i(N_1,c)\leq\frac{1}{2}\sum_{i=0}^{w}\binom{w}{i}\times\left\{\sum_{j=0}^{w-i}(-1)^j\binom{w-i}{j}\left[1+\sum_{l=1}^{\lambda}(-1)^l\binom{i+j}{l}\rho_l\right]^{N_2-1}\right\}\times\left\{1+\sum_{k=1}^{(c+1)i}(-1)^k\binom{(c+1)i}{k}\left[1+\sum_{l=1}^{\lambda}(-1)^l\binom{k}{l}\rho'_l\right]^{N_1}\right\} \quad (8)$$

Fig. 4 shows the upper bound of the performance of a two-level system P_{e1} and P_{e2} as a function of the number of class 1 users, i.e., N_1 along with the simulation results. Note that the number of class 2 users is related to class 1 users simply by the expression $N_2=N-N_1$. For this figure we have $N=20$, the code length $L=80$, the code weight $w=7$ and $\lambda=2$. As it is observed from Fig. 4, P_{e1} remains constant whereas P_{e2} varies as N_2 varies. We have $P_{e2}<P_{e1}$ for $1\leq N_2<N$. The effect of c on P_{e2} is obvious from the figure where P_{e2} is improved considerably as c increases. In this case class 2 users consume higher power when compared to an ordinary one-level FO-CDMA system.

III. Two-level Symmetric Systems

The results of section II indicates that dividing the total number of users in a FO-CDMA network into two classes, each of which having different power levels, there is no change in the performance of lower power users, when compared to one-level systems. However, the performance of higher power users improves and consequently has a better QoS, albeit with increased power consumption. One obvious question that arises here is whether in a given two-level system the performance of the users in both classes can be improved or not. In our follow up discussion we show that indeed it is possible to improve the performance of the users in both classes and the solution is a practical one provided we use advanced binary optical logic gate elements. For the two-level system introduced in section II, the average power consumption per user is given by $P_{av}=\left(N_1P_1+N_2P_2\right)/N$. If we assume that users in both classes are distributed equally, i.e., $N_1=N_2=N/2$, the above expression will be simplified to $P_{av}=\left(P_1+P_2\right)/2$. Furthermore, for $cP_1<P_2\leq(c+1)P_1$ we simply obtain $(c+1)P_1/2<P_{av}\leq(c+2)P_1/2$. Hence,

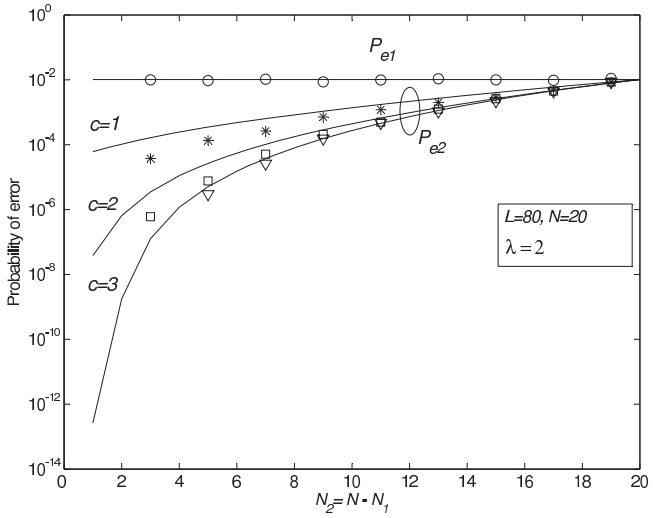

Fig. 4. Probability of error for class 1 and class 2 users for AND logic gate structure FO-CDMA, analytical (upper bound for class 2 users) (solid lines) and simulation (points) results

one can observe that the average power consumption rises when c increases. In what follows we show that using optical logic gates, the multilevel signaling technique introduced in this paper benefits from the performance improvement as we observed in Fig. 4 without a need to increase c and consequently increasing power consumption. For this reason we choose the minimum possible value for c, i.e., $c=1$ and $P_1<P_2\leq 2P_2$. We depict the scheme of the proposed system in Fig. 5. The thresholder block for class 2 users, H_2, remains as before which of course could be modeled as an OR logic gate or equivalently as an optical AND logic gate with one input port. The threshold's value is set at P_2. Therefore H_2 rejects such received chips with power levels less than P_2, evidently including chips with power level P_1. H_1 block, on the other hand, which is placed prior to the class 1 users' corresponding decoders may be designed in such a way that rejects chips with power level P_2. We show the input/output diagram due to such block in Fig. 6. Figure 6 also depicts the implementational scheme of H_1 using optical AND and XNOR logic gates. As we observe from the figure the values of optical logic gates are not the same. To construct a logic gate with variable values using a logic gate with a fixed value one can employ the two following solutions: 1- feeding one input port of the fixed-value logic gate with a constant-power signal. The value of the resulting logic gate is adjusted by tuning the power of the mentioned signal. 2- cascading an optical attenuator or amplifier prior to the fixed-value logic gate. In this case the value of the resulting block is adjusted by the loss (or gain) value of the attenuator (or amplifier).

Since H_1 and H_2, as shown in Fig. 6, reject one level of interference due to the other class, we call such a system, *two-level symmetric one-stage* optical logic gate structure. We can expand upon the above concept if we assume that class 2 users thresholder block, H_2, rejects not only received chips with power level P_1 but also rejects the received chips with power level $2P_1$. In this case many interference patterns due to class 1 users are eliminated. In fact the desired marked chips of a class 2 user are hit by class 1 interfering users

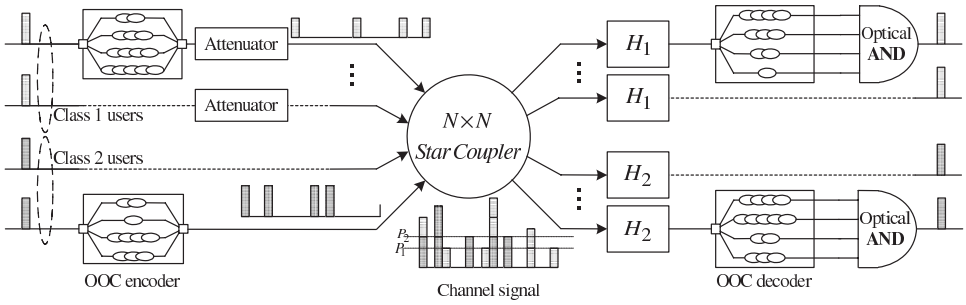

Fig. 5. Two-level FO-CDMA based on advanced binary optical logic gates

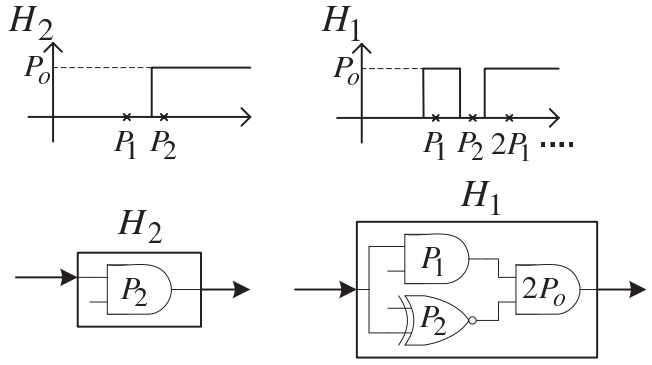

Fig. 6. Thresholder blocks due to class 1 and class 2 users for two-level one-stage system, input/output diagram and implementational architecture

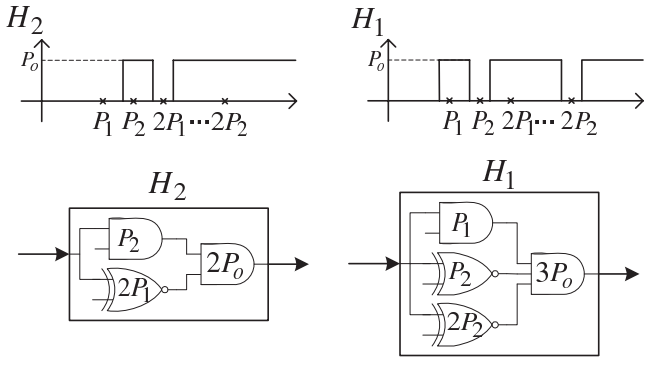

Fig. 7. Thresholder blocks due to class 1 and class 2 users for two-level two-stage system, input/output diagram and implementational architecture

if and only if at least three interfering users from class 1 interfere on the corresponding chip. Similarly, to mitigate the interference of class 2 users on class 1 users, H_1 may reject such chips with power levels P_2 and $2P_2$. Figure 7 shows the input/output diagram and the schematic of H_1 and H_2 for a *two-level two-stage* FO-CDMA receiver. One may intend to reduce MAI between the users of class 1 and the users of class 2 by applying more stages. In this case H_2 rejects chips with power levels P_1, $2P_1$, and $3P_1$ while H_1 rejects chips with power levels P_2, $2P_2$, and $3P_2$ using a combination of AND and XNOR optical logic gates. It is worthy to note that the resolving power of optical logic gates should be considered in the selection of power levels, i.e., P_1 and P_2. We know that the power level of the received optical chips is a linear combination of system's power levels. For example for a *two-level three-stage* system if we have $P_1 < P_2 < 2P_1 < P_1 + P_2 < 2P_2 < 3P_1 < 2P_1 + P_2$ the resolving power of the gates ought to be better than the difference of the above mentioned power levels. In other word in this case the resolving power need to be better than the minimum value of the power levels $(P_2 - P_1)$, $(2P_2 - P_1)$, and $(3P_1 - 2P_2)$. Therefore we can sum up that the depth of interference cancellation, or equivalently the number of stages, depends either on the values of power levels or on the optical logic gates resolving power.

In what follows we derive an upper bound on the probability of error for a *two-level symmetric K-stage* receiver. For such a system an error occurs on the desired user if all the w marked chips are interfered by the users of the same class or the opposite class. Once more we note that the jth marked chip is interfered iff it is hit by at least one user from the same class or it is hit by at least $K+1$ users from the opposite class. Following the discussions in section II if the number of users in the same class is N' then $f_i(N')$ indicates the following probability:

$$f_i(N') = \Pr\big(\alpha_1 = 0, \ldots, \alpha_i = 0, \alpha_{i+1} > 0, \ldots, \alpha_w > 0 \big| N' - 1 \; users \; of \; the \; same \; class\big)$$

and if the number of users in the opposite class is N'' then $g_i(N'', K)$ indicates the following probability:

$$g_i(N'', K) = \Pr\left(\alpha_1 > K, \ldots, \alpha_i > K \big| N'' \; users \; of \; the \; opposite \; class\right)$$

Consequently P_{e1} and P_{e2} is obtained as follows,

$$P_{e1} = \frac{1}{2}\sum_{i=0}^{w}\binom{w}{i} f_i(N_1) g_i(N_2, K) \tag{9}$$

$$P_{e2} = \frac{1}{2}\sum_{i=0}^{w}\binom{w}{i} f_i(N_2) g_i(N_1, K) \tag{10}$$

Where from (4), (5) and (7) we have:

$$f_i(N') = \sum_{j=0}^{w-i}(-1)^j \binom{w-i}{j}\left[1 + \sum_{l=1}^{\lambda}(-1)^l \binom{i+j}{l}\rho_l\right]^{N'-1} \tag{11}$$

$$g_i(N'', K) \le 1 + \sum_{k=1}^{(K+1)i}(-1)^k \binom{(K+1)i}{k}\left[1 + \sum_{l=1}^{\lambda}(-1)^l \binom{(K+1)i}{l}\rho'_l\right]^{N''} \tag{12}$$

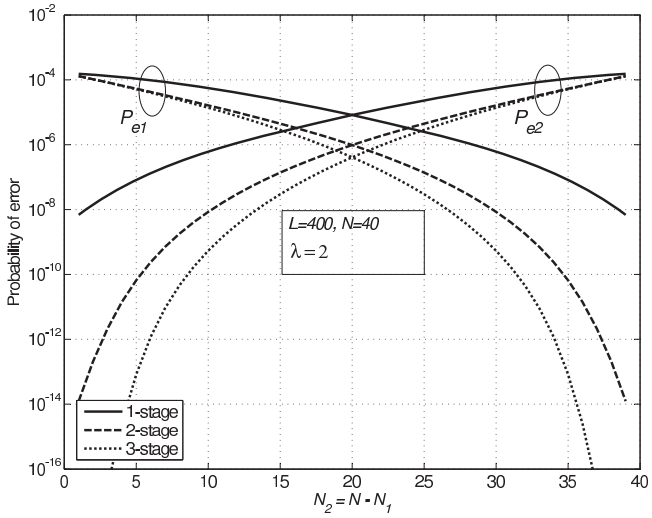

Fig. 8. Probability of error for class 1 and class 2 users vs. number of users in class 1 (or class 2) and number of stages for a symmetric two-level system

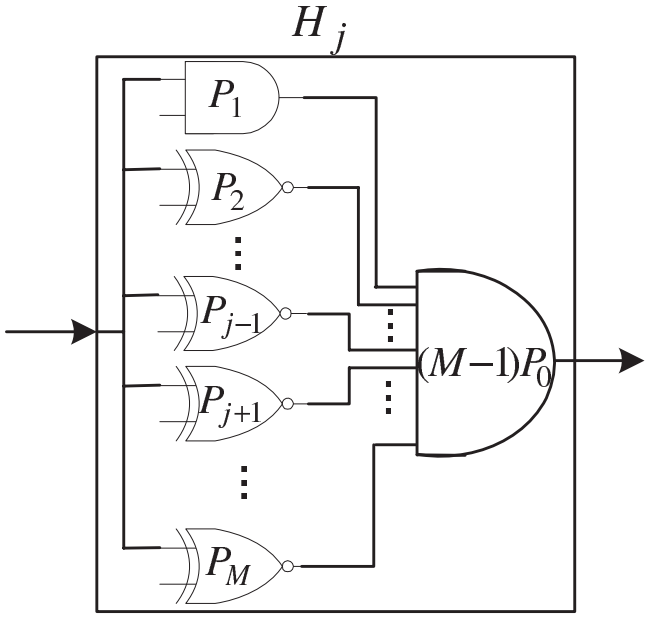

Fig. 9. Thresholder blocks due to class j users for M-level one-stage system, implementational architecture

Figure 8 shows P_{e1} and P_{e2} as a function of N_1 (or N_2) and K. In this figure we have $N = 40$, the code length $L = 400$, the code weight $w = 16$ and $\lambda = 2$. The results are obtained for the worst case scenario from the interference pattern point of view, i.e., when OOC codes are designed such that two different codes interfere in 0 or λ chip positions [7]. From Fig. 8 we observe that when K, the number of the stages, increases the performance of the system is improved. The performance enhancement in this case is due to the reduction of MAI caused by the interfering users of the opposite class. It is worthy to note that the system performance in this case is obtained at no cost in terms of increasing the power level of the desired user but at a cost of higher receiver complexity. However K can not be increased without any restrictions. In Appendix C we obtain the maximum permissible value of K as a function of power levels in use. Another result that is obtained from Fig. 8 is that when the probability of error is set to be better than a predefined value, the maximum number of users that the two-level system can accommodate is maximized when the users are distributed equivalently between the two classes, that is $N_1 = N_2 = N/2$.

IV. Multilevel FO-CDMA Systems

In this section we generalize the proposed model of a two-level system to a multilevel FO-CDMA system. Here we consider an M-level K-stage system where the number of classes is equal to the number of power levels employed, i.e., M. On the other hand K-stage receiver can eliminate up to K interferences caused by the other classes' users in a single chip of the desired user. We assume once again that N active users are communicating through the network and each user can transmit its information with power level P_m where $m = 1, 2, \ldots, M$. Let N_m denotes the number of users that communicate at power level P_m. Evidently we always have $\sum_{m=1}^{M} N_m = N$. Without any loss of generality we assume that $P_1 < P_2 < \ldots < P_M$. Suppose that the desired user has a power level P_j. In a *multilevel one-stage* system the desired user thresholder block which is placed prior to it's corresponding decoder, namely H_j, rejects received chips with power levels $P_1, \ldots, P_{j-1}, P_{j+1}, \ldots, P_M$. Following the discussion in section III this block contains an AND logic gate with value P_1, and $M-2$ XNOR gates with values $P_2, \ldots, P_{j-1}, P_{j+1}, \ldots, P_M$. The output of these $M-1$ gates feed the input of yet another $(M-1)$-input AND logic gate with value $(M-1)P_0$ as shown in Fig. 9. The construction of a *multilevel K-stage* receiver is not straightforward. In this case H_j should reject all received chips with power levels $a_1P_1+a_2P_2+\ldots+a_{j-1}P_{j-1}+a_{j+1}P_{j+1}+\ldots+a_MP_M$ where a_ms are all non-negative integers such that $\sum_{m=1,m\neq j}^{M} a_m = 1$ *or* $2 \ldots$ *or* K. Depending on M and K this linear equation may have many solutions. Though the implementation of such a system especially for large M and K may not be simple still we can obtain the performance of a *multilevel K-stage* system in order to understand its characteristics and operational behavior.

To obtain the probability of error for a *multilevel K-stage* system we use the symmetric property of the system and evaluate P_{ej} which is the probability of error for the users at power level P_j. The solution for multilevel systems is similar to that of two-level systems since in this case the desired user encounters $N_j - 1$ interfering users in its corresponding class and $N - N_j$ interfering users from other classes. The marked chips of the desired user are hit by other classes' interfering users iff at least $K+1$ of these users interfere with the corresponding chips. So similar to eq. (8) we can write,

$$P_{ej} = \frac{1}{2}\sum_{i=0}^{w}\binom{w}{i} f_i(N_j) g_i(N - N_j, K) \qquad (13)$$

where the related functions, f_i and g_i, are obtained from (9).

V. Throughput Analysis

In general the maximum achievable throughput of a network presents a useful view on the operation and the performance of

the corresponding system. In this section we employ throughput as a measure with which we compare the performance of the proposed multilevel FO-CDMA system with the ordinary one-level FO-CDMA system. To obtain the throughput efficiency of a FO-CDMA system we assume that all users communicate with BER $< 10^{-9}$. So for a constant number of users, N, and for a predefined value of λ, e.g., $\lambda = 2$, we need to obtain the minimum possible value for the code length L, and optimum value for the code weight w, such that we first obtain the probability of error to be less than 10^{-9} and secondly the Johnson bound on the number of the codewords i.e., $N \leq \frac{(L-1)\ldots(L-\lambda)}{w(w-1)\ldots(w-\lambda)}$ is to be satisfied [3]. For multilevel systems we assume that users are distributed uniformly among the M classes. In other words we have $N_1 = N_2 = \ldots = N_M = N/M$. Certainly this condition puts a limit on our choice of N and M such that N being multiplicand of M. Eq. (A.5) is used to obtain the probability of error for ordinary one-level FO-CDMA and eq. (13) is used to obtain the upper bound on the probability of error for *multilevel K-stage* FO-CDMA system. For the system considered in this paper the total throughput of the network is proportional to the bit-rate divided by the chip-rate of all the users. So let N/L be the maximum achievable throughput for the system considered in the above discussions.

Figure 10 compares the throughput of a one-level with that of a two-level FO-CDMA system. The results show a considerable improvement for the two-level system. We observe that for $K = 3$, throughput of the two-level system is approximately twice the throughput of the one-level system. The same comparison is presented in Fig. 10 where the throughput of a four-level system is shown along with that of a one-level system. Once again an improvement in throughput efficiency is observed here. It is important to investigate the variations of $g_i(N'', K)$ as a function of K. Based on its fundamental definition the function $g_i(N'', K)$ indicates the effect of other classes' interferences on the desired user. We can show that $g_i(N'', K)$ for high enough values of K is zero for all $i > 0$. To see this mathematically and from appendix B we note that:

$$g_i(N'', K) = \Pr\left(\alpha_1 > K, \ldots, \alpha_i > K | N'' \; users \; of \; the \; other \; classes\right) \leq \Pr\left(\alpha_1 > 0, \ldots, \alpha_{i.K} > 0 | N'' \; users \; of \; the \; same \; class\right)$$

Each interfering user may cause interference on the desired user at maximum λ chips. So if we have $K > N''\lambda$ the upper bound on $g_i(N'', K)$ is equal to zero and consequently $g_i(N'', K) = 0$ for all $i > 0$. This result indicates that we can completely eliminate the interference due to other classes. In other words the users of each class only observe the interfering users of their own corresponding class and the other classes' users do not affect them. Therefore the users of each class are independent from the other classes' users. In this case the throughput of a multilevel system with M power levels is M times of the ordinary one-level system since each class by itself can accommodate the number of users that the one-level system can accommodate.

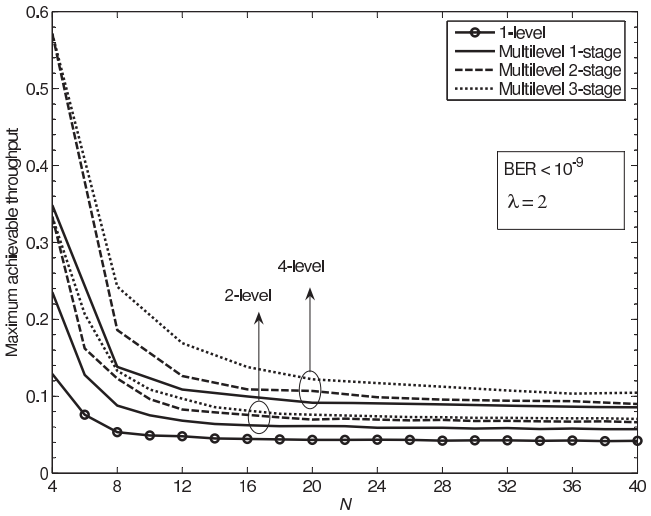

Fig. 10. Maximum achievable throughput for the two-level and four-level systems vs. number of users and number of stages

VI. Conclusion

In this paper we have introduced a new signaling scheme based on power-level division for FO-CDMA communication systems. In this signaling technique we divide network's users into a number of groups. The members within a group transmit their information at the same power level but different from the other groups' members. The receiver design based on optical logic gates not only presents the needed ultra high speed optical processing but also mitigates the multiple-access interference of the undesired users, specifically interfering users from the other groups. In particular we introduced a two-level system in which the members of one group gain an improvement in QoS at the cost of consuming higher power when compared to the other classes' users. The receiver design of such system does not differ from the well known AND logic gate structure for FO-CDMA systems. On the other hand we show that using a special combination of optical OR, AND, and XNOR logic gates at the receiver end prior to the corresponding decoder we can improve the performance of all classes' users without a need to increase power consumption. Such a design leads to increasing the throughput of the network which we show to be proportional to the number of power levels used in the system.

Appendix A

If L, λ, w and N denote code length, code weight, cross-correlation coefficient and the number of users respectively, the probability of error caused by MAI is obtained as follows,

$$P_e = \frac{1}{2}\Pr\left(error|1\right) + \frac{1}{2}\Pr\left(error|0\right)$$

Neglecting shot noise the first term on the right hand side of the above equation is equal to zero. An error is occurred, by the MAI noise, only when the transmitted bit is 0. If we show the number of interference on the ith marked chip of the desired OOC by α_i according to Fig. 2 the probability of

error is as follows [7],

$$P_e = \frac{1}{2}\Pr(error|0) = \frac{1}{2}\Pr(\alpha_1 > 0, \alpha_2 > 0, \ldots, \alpha_w > 0)$$
$$= 1 - \Pr(\alpha_1 = 0 \ or \ \alpha_2 = 0 \ or \ldots or \ \alpha_w = 0)$$
$$= 1 + \sum_{k=1}^{w}(-1)^k \binom{w}{k} \Pr(\alpha_1 = \alpha_2 = \ldots = \alpha_k = 0) \quad \text{(A.1)}$$

Note that the maximum allowable cross-correlation coefficient for our OOC set is λ. Let $p_1, p_2, \ldots,$ and p_λ denote λ parameters each defined as follows: p_1 is the probability that one interfering user hits on just one specified chip pulse position of the desired user's OOC. p_2 is the probability that it hits on exactly two specified chip pulse positions of the desired user's OOC and so on. In an OOK OCDMA system the following relation is valid for the interference probabilities [7]:

$$\sum_{k=1}^{\lambda} k\binom{w}{k} p_k = \frac{w^2}{2L} \quad \text{(A.2)}$$

With the above definition, the λ events that are related to $p_1, p_2, \ldots,$ and p_λ are disjoint. Furthermore all $N-1$ interfering users are independent and hence we can write:

$$\Pr(\alpha_1 = \alpha_2 = \ldots = \alpha_k = 0) = \left[1 + \sum_{l=1}^{\lambda}(-1)^l \binom{k}{l}\rho_l\right]^{N-1} \quad \text{(A.3)}$$

where we have defined:

$$\rho_l = \Pr(\alpha_1 = \ldots = \alpha_l = 1 | one \ interfering \ user) =$$
$$p_l + \binom{w-l}{1} p_{l+1} + \ldots + \binom{w-l}{\lambda - l} p_\lambda = \sum_{i=l}^{\lambda} \binom{w-l}{i-l} p_i \quad \text{(A.4)}$$

Substituting (A.4) in (A.3) and using (A.2) we can rewrite (A.1) as follows:

$$P_e = \frac{1}{2}\left\{1 + \sum_{k=1}^{w}(-1)^k \binom{w}{k} \times \left[1 + \sum_{l=1}^{\lambda}\sum_{i=l}^{\lambda}(-1)^l \binom{k}{l}\binom{w-l}{i-l} p_i\right]^{N-1}\right\} \quad \text{(A.5)}$$

However it is shown that if OOC codes are chosen such that $p_k = 0$ for $1 \le k \le \lambda - 1$ and thus only $p_\lambda \neq 0$, we obtain an upper bound on the performance of such an OCDMA system with generalized OOCs.

APPENDIX B

In this appendix we obtain expressions (4) and (6). From (2) we have:

$$f_i(N_2) = \Pr\big(\alpha_1 = 0, \ldots, \alpha_i = 0, \alpha_{i+1} > 0, \ldots, \alpha_w > 0 \big| N_2 - 1 \ class2 \ users\big) - \Pr\Big[(\alpha_1 = 0, \ldots, \alpha_i = 0) and (\alpha_{i+1} = 0 \ or \ \alpha_{i+2} = 0 \ldots or \ \alpha_w = 0) \big| N_2 - 1 \ class2 \ users\Big] \quad \text{(B.1)}$$

From the well-known property of the probability of the union of events with the aid of the probability of their mutually exclusive events we can write:

$$f_i(N_2) = \Big[\Pr\big(\alpha_1 = \ldots = \alpha_i = 0 \big| N_2 - 1 \ class2 \ users\big) - \sum_{j=1}^{w-i}\Pr\big(\alpha_1 = \ldots = \alpha_i = \alpha_{i+j} = 0 \big| N_2 - 1 \ class2 \ users\big) + \frac{1}{2!}\sum_{j,j'=1|j\neq j'}^{w-i}\Pr\big(\alpha_1 = \ldots = \alpha_i = \alpha_{i+j} = \alpha_{i+j'} = 0 \big| N_2 - 1 \ class2 \ users\big) - \ldots\Big] = \sum_{j=0}^{w-i}\binom{w-i}{j}\Pr\big(\alpha_1 = \ldots = \alpha_{i+j} = 0 \big| N_2 - 1 \ class2 \ users\big) \quad \text{(B.2)}$$

To obtain inequality (6) we first assume the number of interferences on the ith chip of the desired user as α_i. It is evident that each interfering user can not hit on a single marked chip of the desired user more than once. To evaluate $\Pr(\alpha_1 > c, \ldots, \alpha_i > c)$ one can assume that there are at least $(c+1) \times i$ interfered chips containing i columns and each column with at least $c+1$ interfered chips. To obtain an upper bound on $\Pr(\alpha_1 > c, \ldots, \alpha_i > c)$, we can rearrange the interfered chips vertically and find the probability that they are interfered at least by one marked chips of the interfering users. By doing so we can write:

$$\Pr\big(\alpha_1 > c, \ldots, \alpha_i > c\big) \le \Pr\big(\alpha_1 > 0, \alpha_2 > 0, \ldots, \alpha_{(c+1)i} > 0\big) \quad \text{(B.3)}$$

One can check that the right-hand side of the above inequality is similar to the expression in (A.1) and thus can be obtained by following the approach presented in Appendix A but with a change in the code weight of the desired user. In this case we denote the code weight of the interfering users by w and the code weight of the desired user by $w' = (c+1)i$. Using the same definition on $p'_1, p'_2, \ldots,$ and p'_λ as in Appendix A we can rewrite (A.2) as:

$$\sum_{k=1}^{\lambda} k\binom{w'}{k} p'_k = \frac{ww'}{2L} \quad \text{(B.4)}$$

Using (A.3)-(A.5) we have:

$$\Pr(\alpha_1 > c, \ldots, \alpha_i > c) \le \Pr\big(\alpha_1 > 0, \alpha_2 > 0, \ldots, \alpha_{(c+1)i} > 0\big) = 1 + \sum_{k=1}^{w'}(-1)^k \binom{w'}{k}\left[1 + \sum_{l=1}^{\lambda}(-1)^l \binom{k}{l}\rho'_l\right]^{N-1} \quad \text{(B.5)}$$

where $\rho'_l = \sum_{j=l}^{\lambda}\binom{w-l}{j-l}p'_j$.

APPENDIX C

In this appendix we obtain the maximum allowable number of stages, K, for a two-level system. Assume that the minimum resolving power of the optical logic gates is P_b. For a two-level system we choose P_1 and P_2 as an integer multiple of P_b. Let $P_1 = A_1 P_b$ and $P_2 = A_2 P_b$ with A_1 and

A_2 as the positive integers and $A_1 < A_2$. The power level of the received optical chips is a linear function of P_1 and P_2. Therefore each received chip's power level value can be written as $P_R(a_1, a_2)=a_1P_1+a_2P_2=(a_1A_1 + a_2A_2)\,P_b$ with a_1 and a_2 as the non-negative integers. In a *two-level K-stage* system H_1 rejects received chips as $P_R(0, a_2)$ and H_2 rejects received chips as $P_R(a_1, 0)$ for $a_1, a_2 \leq K$. The proper operation of H_1 is guaranteed if $P_R(0, a_2) \neq P_R(b_1, b_2)$ for all $(b_1, b_2) \neq (0, a_2)$ where b_1 and b_2 are non-negative integers not greater than K. Otherwise we have $a_2P_2=b_1P_1+b_2P_2$ and consequently $(a_2 - b_2)A_2=b_1A_1$ for some a_2, b_1 and b_2. In this case we have $\frac{b_1}{a_2-b_2}=\frac{A_2}{A_1}=\frac{A'_2}{A'_1}$ where $A_1 = A'_1 \times greatest\ common\ divisor(A_1, A_2)$ and $A_2 = A'_2 \times greatest\ common\ divisor(A_1, A_2)$. Evidently A'_1 and A'_2 are mutually prime. So the minimum possible value for b_1 in order to satisfy the above fractional equation is equal to A'_2. One can deduce that for all $b_1<A'_2$ the above fractional equality has no answer and thus the proper operation of H_1 is guaranteed. Because of the symmetry, for all $b_2<A'_1$ the proper operation of H_2 is also guaranteed. Since we have assumed $A'_1<A'_2$ it is sufficient to have $K<A'_1$ for the proper operation of *two-level K-stage* systems. One can check that choosing A_1 and A_2 such that $greatest\ common\ divisor(A_1, A_2) = 1$ increases the largest permissible value of K.

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