Applications and Performance of Optical Analog-to-Digital Converter and Optical Logic Gate Elements in Multilevel Multiclass Fiber-Optic CDMA Systems

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***Abstract*—In this paper, we present and analyze a novel all-optical multilevel multiclass optical code division multiple access (OCDMA) system, using optical analog-to-digital converter (ADC) and advanced optical logic gate elements. In such OCDMA network, users are distributed in M different classes. Furthermore, power level with which users in class j, $j = 2, \ldots, M$, transmit optical pulses, is twice the power level at which users of class $j-1$ transmit their optical pulses. We achieve optical transmitter structure that satisfies these conditions using power control schemes. Also, we suggest two receiver structures for the aforementioned multiclass multilevel system. The first and simple receiver structure is based on optical AND logic gate elements. The second structure uses an optical ADC as well as optical AND logic gates. We obtain the performance for the aforementioned two types of receivers and compare their results with the traditional one-level OCDMA system. We show that using the proposed multilevel multiclass scheme improves system performance considerably by means of decreasing error probability as well as increasing the network capacity.**

***Index Terms*—Multiclass, mutilevel signaling, optical analog-to-digital converter (ADC), optical code division multiple access (OCDMA), optical logic gates.**

I. Introduction

With advances in optical communication devices and subsystems, as well as the need to make all-optical communication networks, attempts have been made to produce digital optical systems in order to perform advanced network functionalities in routing, switching, and access systems. In the optical access systems, the optical designer must provide the best-suited multiple access scheme in order to meet the application-specific requirements. Among many multiple access techniques, optical code division multiple access (OCDMA) has been receiving a great deal of attention due to its robust and flexible functionality, soft capacity handling, and security potentials [1]–[9]. Furthermore, taking the advantages of advanced optical devices, such as optical analog-to-digital converter (ADC) and optical logic gate elements, one can design and devise multilevel multiclass OCDMA systems.

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Recently, several multilevel signalings for use in OCDMA networks to improve the performance and spectral efficiency have been proposed [3]–[5]. In this paper, a new multiclass OCDMA fiber-optic access network based on optical orthogonal codes (OOC) and multilevel signaling is introduced. Employing advanced optical devices, such as optical logic gate elements and optical ADC technology facilitates, using multilevel signalings in OCDMA systems [10]–[13]. This not only allows a further increase in capacity compared to the traditional OCDMA systems, but also provides multiple class of users with different QoS.

A multilevel signaling in which a predefined power level assigned to each class of users is proposed in [3]. In this paper, the performance and also the all-optical receiver structure, which is based on optical logic gate elements were proposed and studied. It was indicated that if the power levels in use for M classes are $a_1P, a_2P, \ldots, a_MP$, where $a_1, a_2, \ldots, a_M$ are integer numbers, the performance of the system is maximized if the greatest common divisor of $a_1, a_2, \ldots, a_M$ is one. The main focus was on two-level systems, i.e., $M = 2$ in [3]. However, even though the performance for the multilevel systems was obtained, but it was indicated that the implementation of such systems with more than two levels of power, using the proposed receiver structure designed based on XNOR and AND logic gate elements is quite complex.

Using power rejection property of the optical XNOR in [3], a multistage receiver structure that rejects the received optical chips of the opposite classes was highlighted. In this paper, however, we propose using optical ADC as the core of all-optical receiver structure. We categorize all users to M classes. Users belonging to class j transmit at power $2^{j-1}P$ for $j = 1, \ldots, M$. We propose the structure of the corresponding transmitter and receiver, as well as study their performance. We show that the proposed technique improves the system performance by increasing the capacity as well as decreasing the error probability. Using this technique, users of different classes obtain different QoS.

The rest of the paper is organized as follows. In Section II, we present the basic concepts of the new multilevel OCDMA system. In Section III, we describe the system model and introduce a new structure for transmitter, and a new structure for the receiver based on optical ADC. In Section IV, we study the model of mutual interference between different classes. In Section V, we obtain the performance of the system considering

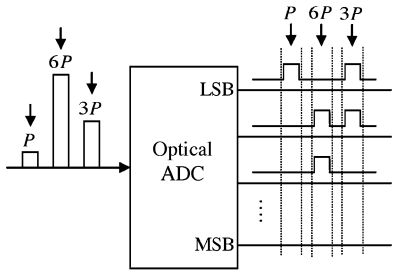
the generalized form of OOCs. In Section VI, we present the results and some discussions. Section VII concludes the paper.

II. Basic Concepts

In a typical OCDMA system, investigating the effect of its multiple access interference, is directly related to the entanglement of some binary "0" and "1" pulses on each other. For the best receiver structures, in OCDMA systems, i.e., AND logic gate and chip-level detector structures, one hit or more from undesired users chips can flip a "0" chip to a "1" chip, erroneously. As a consequence in these receiver structures with OOK signaling only, a flip from chip "0" to chip "1" can occur. We propose and study a novel multilevel technique for OCDMA systems in [3], where we categorize all users into different classes. Users belonging to each class transmit at a specified power level. In this paper, however, we introduce a new set of power-level assignment scheme that helps to simplify the detection of the desired signal in an OCDMA system. We study and investigate the effect of such a multilevel signaling from OCDMA point of view. We note that by assigning different power levels to various classes of users, then the effect of multiaccess interference (MAI), substantially differs from the traditional one-level OCDMA multiple access systems. In particular in [3], it is shown that with a multilevel signaling and proper receiver structures, receivers belonging to one class of level (power) can eliminate the MAI of other classes, considerably. Hence, with this perspective, interclass interference and intraclass interference have two different effects. As we discuss in [3], in the ideal case, ignoring the complexity of the receiver structure, one can ideally eliminate interclass interference to almost zero. This implicates that various classes have no interference on each other. Hence, in this case, for a system with M classes, the capacity can be M times higher than the capacity of a one-level single-class OCDMA system. The main receiver structure proposed in [3] is based on optical logic gate elements, such as XNOR and AND gates. Furthermore, we show that the proposed structure is simple and operates well for a two-level system, while for M-level $M > 2$ systems, the receiver structure can prove to become extremely complex and complicated from implementation point of view. In this paper, we propose an alternative receiver structure based on optical ADC for two purposes. First, ADC operates extremely well for a multilevel system with $M > 2$, and second ADC rejects the interclass interference as we elaborate and reason in the following.

Assume that we have two classes of users. Users of class 1 transmit at power level P and users of class 2 transmit at power level $2P$. We consider a chip-synchronous case and an additive optical channel. In the following, we show that using an ADC in the receiver structure, no class 2 user may make interference on a class 1 user. One can consider that if we have one class 1 user transmitting bit d_0 and I_2 class 2 users simultaneously hitting on one marked chip of the desired class 1 user, then the received power level due to the interfered chip is as follows:

$$P_r = d_0 P + 2\sum_{j=1}^{I_2} b_j P \tag{1}$$



Input Power	Output Bits
0	00...000
P	00...001
$2P$	00...010
$3P$	00...011
$4P$	00...100
⋮	⋮

Fig. 1. Output–input relation of ADC.

where b_j denotes the data bit of the jth interfering user from class 2. The linear gain at the receiver is set such that the received signals with power level P is mapped on the LSB of ADC. In this case, the relation between the input power level and output bits generated by ADC can be depicted as in Fig. 1. Hence, when the optical pulse with power level as defined in (1) is applied to ADC, the LSB is equivalent to d_0, since the second term of (1) is always an even multiple of P. This implies that b_j, $j = 1, \ldots, I_2$, due to MAI of class 2 users do not affect on the output LSB of ADC. In other words, the hits form undesired users from class 2 cannot make any interference on the desired class 1 marked chip. In this case, we do not have interclass interference from the higher class users on the lower class users.

On the other hand, we need to study the intraclass interference effect for class 1 users. Again, if we let d_0 denote the bit information of the desired user and d_j, $j = 1, \ldots, I_1$, the bit information due to class 1 interference users that hit on the desired marked chip, the received power of the desired marked chip is as follows:

$$P_r = d_0 P + \sum_{j=1}^{I_1} d_j P = d_0 P + D_{I_1} P. \tag{2}$$

One can check that if D_{I_1} is an even number, it does not affect the LSB, but if it is an odd number, then it causes interference on the desired chip, since it may convert the LSB from "0" to "1" or from "1" to "0" depending on the bit information d_0. In this case, if $d_0 = 0$, then receiver detects the marked chip as "1" erroneously and *vice versa*. But if D_{I_1} is an even number $2K$, it does not change d_0. We can explain this effect as follows: when two ON or pulsed chips from two class 1 interfering users simultaneously hit on a desired marked chip, then they form a single ON chip that can be considered as an interfering chip belonging to class 2. Hence, it does not affect class 1 desired chip as we described earlier. In the generalized case, when we have $2K$ ON class 1 interfering chips each with power level P, then they are equivalent to K ON chips each with power level $2P$, hence there would be no interference on the hit marked chip of class 1 desired user. On the other hand, for odd values of D_{I_1}, if we have $2K + 1$ ON class 1 interfering chips, it is then like K class 2 users and one class 1 interfering user that can cause chip pulse conversion at the output of ADC.

In the following, we consider that the desired user is a class 2 user with power level $2P$. The intraclass interference in this case is same as we explained for class 1 users. However, the effect

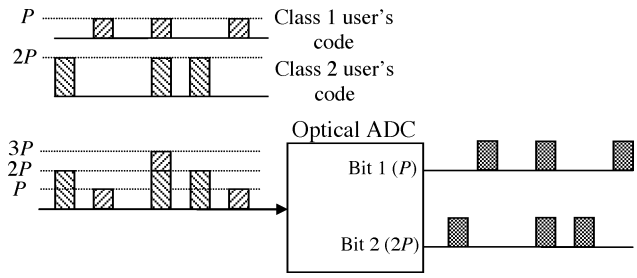


Fig. 2. ADC operation for a two-class two-level OCDMA system.

of interclass interference form class 1 on class 2 differs from the effect of class 2 on class 1 users. One can check that two simultaneous hit from the lower class users with power level P is equivalent to one hit with power level $2P$, and hence, it can be considered as an interference from class 2. In this case, one can observe that in the special cases, lower class users can make interference on the higher class desired user mark chips.

Fig. 2 shows a simple example of the operation of ADC in a two-class two-level OCDMA system. A class 1 user with power level *P* and a class 2 user with power level 2*P* are present. The summation of both users' corresponding codes enters to the ADC. Such pulses with power level *P* are mapped on the first bit of ADC. In this case, ADC separates chip stream belonging to class 1 and class 2 users on its first and second output bits, respectively.

In Section IV, we present a mathematical analysis that provides the probability of interclass and intraclass interference for the general multilevel systems. In this general form, we have M classes and users belonging to class j, $j = 1, \ldots, M$, transmit at power level $2^{j-1}P$.

III. OCDMA Multilevel Multiclass System Description

For our system description, we have $N + 1$ users, where each user communicates using an associated OOC. In this case, an OOC set with $N + 1$ codes is needed. We assume the length, the weight, and the crosscorrelation of codes are L, w, and λ, respectively. We begin by categorizing the users into M different classes and let N_j denote the number of users belonging to class j, such that $\sum_{j=1}^{M} N_j = N + 1$ for $1 \leq j \leq M$.

A. Transmitter: All-optical Multilevel Multiclass Encoder

The optical transmitter we propose is based on a passive star architecture with two level of hierarchies as shown in Fig. 3. A passive optical combiner is assigned to each class in order to combine the signal of each users belonging to the corresponding class. The combined signal is forwarded into a fiber medium through the optical combiner. We need to have the power level of each user's optical pulses belonging to class j be equal to $2^{j-1}P$ for $j = 1, \ldots, M$, where P is the average output power of class 1 users. We assume that a control signal from the downstream performs the power control of the upstream power flow. Several methods have been proposed for power control in passive optical network (PON) upstream [14], [15]. As shown in Fig. 3, all users' combined optical signal is present at the output fiber within which the power level of optical pulses due to class j is half of the optical pulses due to class $j + 1$. We propose and study two types of receiver structures, obtain their performance, and compare their behavior by evaluating their error probability.

B. AND *Logic Gate Receiver Structure*

Fig. 4 shows a typical receiver structure based on optical AND logic gate element. In this type of receiver, an optical hardlimiter is placed following the amplifier. The optical data stream at the amplifier output is sent to M branches using an optical splitter. We assume that the optical amplifier gain compensates for all losses due to path between transmitter and receiver, and also the loss due to postoptical splitters. In this case, the optical amplifier's gain is set such that the received power of class j users' chips at the output of the first stage optical splitter is equal to the power of the transmitted chips of the same class, i.e., $2^{j-1}P$.

Each branch with its own *unique* optical hardlimiter is affiliated to a class. We choose the threshold value of optical hardlimiter for class j users to be equal to the power level of its corresponding class, i.e., $2^{j-1}P$. Therefore, the optical hardlimiter of class j eliminates optical pulses with power level less than $2^{j-1}P$, and also the same hardlimiter clips the optical pulses with power level equal or more than $2^{j-1}P$. Following the hardlimiter, we use a second stage optical splitter for each class in order to split the signal of users belonging to the corresponding class. The related OOC decoder for each user consisting of fiber-tapped delay lines is placed at the output of the splitter. The optical AND logic gate element decides on the transmitted bit, i.e., bit "1" is detected if all marked chips are ON, otherwise "0" is detected.

C. Optical ADC Receiver Structure With AND Logic Gate

Fig. 5 shows a typical optical ADC receiver structure with AND logic gate. The received optical stream is forwarded to the optical ADC through an optical amplifier with adjustable gain. The gain of this optical amplifier is adjusted in such a way that the power level due to class 1 users, i.e., P is mapped on the LSB of ADC. As a consequence and for an ideal case, the output bits of ADC follows the values shown in Fig. 1 versus the input received power. The LSB of ADC is connected to the star coupler of class 1. The next output branch of ADC is assigned to class 2, etc., as shown in Fig. 5. The output of the OOC decoder, which counts the number of ON marked chips is compared to a threshold TH.

In this receiver structure, we use the optical ADC to distinguish the optical signal of each class. Users of class 1 take the optical chip stream on the LSB of ADC. Likewise, class j users take the data stream on the jth branch of the ADC output port. Due to intrinsic property of ADC, two kinds of error may occur on the marked chips. Just like the conventional OCDMA systems, an interference may convert an OFF chip to an ON chip. Assume a marked chip of a class 1 user to be OFF. If another class 1 user make a hit on this marked chip, a conversion from chip "0" to chip "1" occurs. On the other hand, assume that a

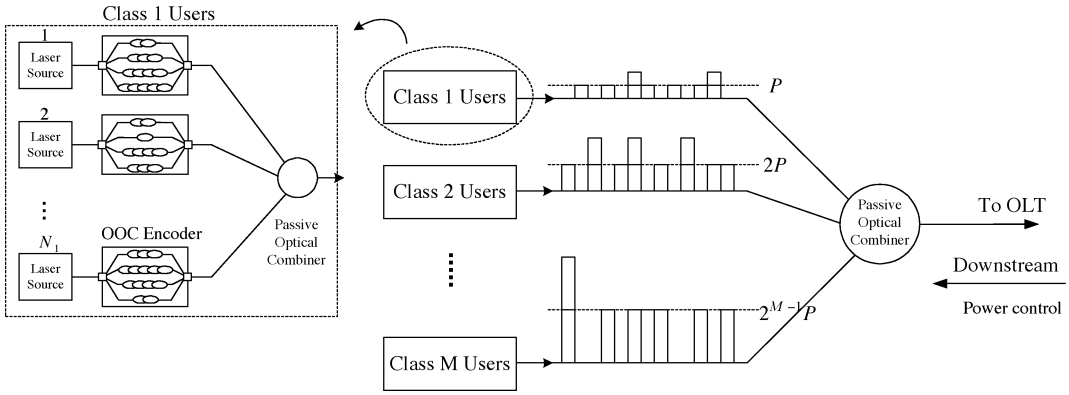


Fig. 3. All-optical transmitter structure for the proposed multilevel multiclass OCDMA system.

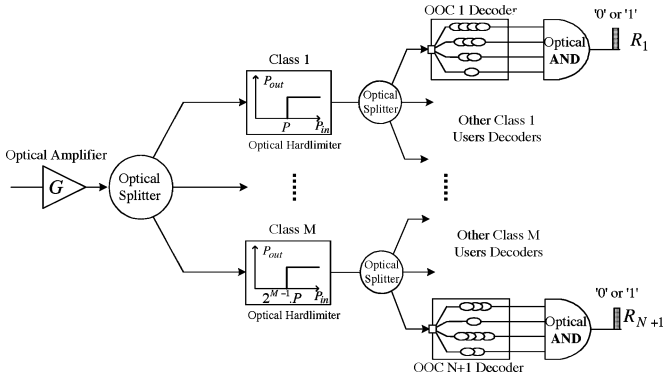


Fig. 4. Optical AND logic gate receiver structure for a typical multilevel OCDMA system.

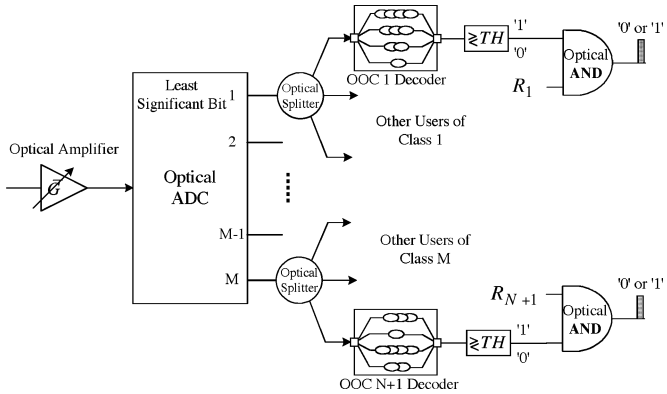


Fig. 5. Optical ADC receiver structure with optical AND logic gate for a typical multilevel OCDMA system. R_1 to R_{N+1} come from the structure of previous figure.

marked chip of the class 1 user is ON, i.e., its power level is P. If another class 1 user make a hit on this marked chip, i.e., an optical pulse with power level P, the power level of interfered chip becomes $2P$, and according to Fig. 1, the LSB of ADC generates "0" for this chip. In this case, a conversion from chip "1" to chip "0" occurs.

The motivation behind using ADC in the aforementioned receiver structure is in its high ability to reject the power levels belonging to opposite classes. First of all, we note that the jth output port of ADC does not contain any information on the higher classes, i.e., classes $j+1, \ldots, M$. Therefore, at the output of ADC, there are no interference from the higher classes on lower class users. On the other hand, one can check that no single hit from lower classes can make interference on the higher class users. For instance, at least two simultaneous hit from class $j-1$ users on a single marked chip of class j user can cause interference on this marked chip. To improve the error probability, we can use the structure of Fig. 4 in parallel with the ADC structure. We know that in the AND logic gate structure transmitted bit, "1" is detected correctly and only transmitted bit "0" can be affected by MAI. Therefore, in the AND logic gate structure only error conversion from bit "0" to "1" may occur, and consequently, R_1 to R_{N+1} are never detected "0" erroneously. Regarding this fact, if we perform AND logic between the outcome of the structure of Fig. 4, i.e., R_1 to R_{N+1}, and the corresponding outcome of ADC receiver structure, as shown in Fig. 5, the probability of error will not be worsen than the case when a single ADC is in use. However, we can show that it can improve the performance for some especial cases. For example, assume that the transmitted bit of the desired user is "0" and w_I chips out of w marked chips of desired user are hit by interfering users and $\mathrm{TH} < w_I < w$ (we will show that the optimum threshold is around $w/2$). In this case, the ADC receiver decides on "1" erroneously (since $w_I > \mathrm{TH}$), but AND logic gate receiver decides on "0" (since $w_I < w$). The outcome of the last AND gate is "0" and that is a correct decision.

IV. Multilevel, Multiclass OCDMA Interference Analysis

To obtain the performance of the aforementioned proposed receivers, it is first necessary to study and investigate the interfering signal.

A. AND *Logic Gate Receiver Structure*

In this receiver structure, for each class, we are facing two types of interferences. Assume the desired user is in class j, then the two types of interferences include interferences from lower classes, i.e., classes $1, \ldots, j-1$, and the interferences from the same class and higher classes, i.e., classes $j, \ldots, M$. Note that on one hand in the case, where an interfering user from the same class or higher classes hits on the marked chip of

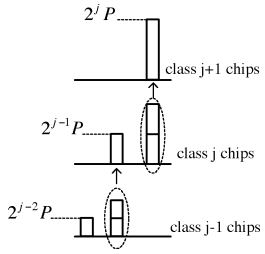


Fig. 6. Jumping model of interference chips from a lower class to higher class.

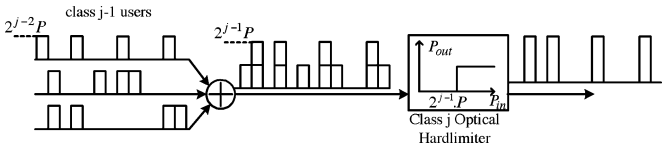


Fig. 7. Effect of interfering users from class $j-1$ on class j receiver.

the desired user, it causes an interference on this marked chip. On the other, at least 2^m chips from the users of class $j-m$ need to hit simultaneously on the marked chip of a class j user to cause an interference on this marked chip. As a matter of fact, a combination of hits due to all lower class users can make interference on the higher class user. To simplify the problem, we show the effect of lower classes' interference on the higher classes in Fig. 6, where two hits of class $j-1$ users result into a hit in class j, and similarly, two hits of class j users can be considered as a hit in class $j+1$.

To obtain an estimation for lower classes' interference, we have shown the transmission of interference between different classes in Fig. 6. To obtain the exact probability of interference in this case could prove to be mathematically tedious and complex. To simplify and overcome mathematical complexity, we present an approximation as follows. A single chip of a class $j-1$ user with power level $2^{j-2}P$ is less than the threshold value of class j receiver, i.e., $2^{j-1}P$, as shown in Fig. 7. As a consequence, it gets eliminated as an interference. Therefore, from a class j user point of view, if for example, two class $j-1$ users, simultaneously hit a chip position, this chip position can make interference on the class j users. Therefore mathematically, assuming two users from class $j-1$, the mean number of interfered chips is equal to $w^2/2L$. If we intend to consider the worst case scenario, i.e., we assume that each pair of class $j-1$ users hit on distinct chips, we can write the mean number of chips that mutually hit upon each other in class $j-1$ as $\binom{n_{j-1}}{2} w^2/2L$. Without any loss of generality if we assume that users of class $j-1$ are synchronous, we can say that in the worst case if we observe the accumulated optical stream deduced from class $j-1$ users in a window with length equal to L chips, then $\binom{n_{j-1}}{2} w^2/2L$ chips are interfered. Thus, on average a higher class user sees $\binom{n_{j-1}}{2} w^2/2L$ chips in a bit duration from the lower class users. To simplify the analysis, we model the contributed hits from the lower classes by an extra number of users in the same class, i.e., N_{eff_j}. We define N_{eff_j} as the effective number of interfering users from class $j-1$ on class j. Since, the code weight is w, we can approximate N_{eff_j} by dividing the number of contributed hits from the lower class on w

$$N_{\text{eff}_j} = \begin{cases} \frac{w.n_{j-1}(n_{j-1}-1)}{4L}, & j \geq 2 \\ 0, & j = 1 \end{cases}. \tag{3}$$

As a matter of fact N_{eff_j} users obtained from (3) do not satisfy the OOC codes conditions. However, we will show by simulation results that this approximation does not affect the accuracy of analysis. n_j in (3) is the accumulate number of interfering users in each class, i.e., the addition of interfering users of class j itself and the interfering users from the lower classes. In this case, we have

$$n_j = \begin{cases} N_j + N_{\text{eff}_j}, & j \geq 2 \\ N_1, & j = 1 \end{cases} \tag{4}$$

(3) and (4) give us the effective number of lower classes' interference users for each class.

B. ADC Structure With AND *Logic Gate Using Binary Pulse-Position Modulation*

With respect to ADC in Section II, we discussed two types of conversion, namely, ON chip to OFF chip and OFF chip to ON chip, due to intrinsic property of ADC. In analyzing ADC, we may assume bit "1" and bit "0" as the vectors of marked chips. For instance, in OOK signaling bit "0" and "1" can be represented as $v_0 = (\underbrace{00\ldots0}_{w})$ and $v_1 = (\underbrace{11\ldots1}_{w})$, respectively. In this case, the hamming distance between v_0 and v_1 is equal to w. Therefore, $\lceil w/2 \rceil$ conversion of ON and OFF chips is sufficient to cause an error. In this case, TH in Fig. 5 is set to $w/2$. To simplify and also improve the performance, we choose binary pulse-position modulation (BPPM) signaling in which bit "0" and bit "1" can be represented as $v_0 = (\underbrace{11\ldots1}_{w}\underbrace{00\ldots0}_{w})$ and $v_1 = (\underbrace{00\ldots0}_{w}\underbrace{11\ldots1}_{w})$, respectively. The hamming distance of v_0 and v_1 in this case is equal to $2w$. We set TH in Fig. 5 equal to w. Therefore, if there is a type of interference that converts OFF chip to ON chip and *vice versa*, w interferences are sufficient to make an error on the transmitted bit. We call this kind of interference type I interference. Another kind of interference that only make a conversion from chip "0" to chip "1" is called type II interference. This type of interference is similar to the interference in the conventional one-level OCDMA systems. We will show that the higher class's users can only make type II interference on lower class's users.

For our analysis, we consider BPPM signaling. For the receiver structure shown in Fig. 5 and assuming that the transmitted bit is "1", an error occurs on a class j desired user if: 1) all first w marked chips of the desired user are hit by chip pulses with power level equal or more than $2^{j-1}P$; and 2) at least w out of $2w$ marked chips of the desired user are hit by type I interference. Let us begin by a class 1 user as the desired user. One can check that users from all other classes, namely classes $2, 3, \ldots, M$, do not cause type I interference on the class 1 desired user. To check this, assume that K_i, $i = 2, 3, \ldots, M$, users from class i hit on a marked chip of the desired user. The interference power level then is $\sum_{i=2}^{M} K_i 2^{i-1} P$, which is

always an even multiple of P. Therefore, it could not affect the LSB port of ADC. Now we assume a class j user. If we denote by K_i, $i = j+1, \ldots, M$, the number of interfering users from higher classes then the contributed interference power level is $\sum_{i=j+1}^{M} K_i 2^{i-1} P = 2^j \sum_{i=j}^{M-1} K_i 2^{i-j} P$ that does not affect jth port of ADC. As a consequence, the users of higher classes cannot make type I interference on class j users, i.e., the users of classes $j+1, \ldots, M$, cannot cause type I interference on the users of class j.

However, the users of the same class may cause type I interference upon each other. Furthermore, the users of lower classes too, may cause type I interference on a higher class user if their interference takes place in class j according to the model shown in Figs. 6 and 7. Therefore, by using (3) we can express the number of type I interfering users of class j as follows:

$$n_j = N_{\text{eff}_j} + N_j = \frac{w n_{j-1}(n_{j-1}-1)}{4L} + N_j \tag{5}$$

with $N_{\text{eff}_1} = 0$ and $n_1 = N_1$. However, all other users belonging to higher classes are potentially type II interfering users. Therefore, the number of type II interfering users is as follows:

$$n'_j = \sum_{i=j+1}^{M} N_i. \tag{6}$$

V. Performance Analysis With BPPM

We consider BPPM signaling for data transmission. In this case, the data stream sent by user k in class j can be written as follows:

$$s_k^{(j)}(t) = \sum_{i=-\infty}^{+\infty} 2^{j-1} P C_k(t - b_i T_b - 2iT_b) \tag{7}$$

where $C_k(t)$ is the OOC code assigned to user k with duration T_b, $b_i \in \{0,1\}$ is the ith information bit. Therefore, each bit duration in BPPM is equal to $2T_b$ if $b_i = 0$, the OOC code is sent in the first T_b duration and if $b_i = 1$, the OOC code is sent in the second T_b duration. In order to analyze the performance in this case, we only consider multiple access interference, which is the dominant noise in OCDMA systems. This gives us the floor on the error probability or equivalently the maximum achievable performance of the system when OSNR is sufficiently high.

A. AND Logic Gate Receiver Structure

For the performance analysis, we begin by a desired user in class 1. For the bit error rate (BER) evaluation in BPPM signaling, we assume that bit "1" is sent, so an error occurs if all the first w marked chips are hit by interfering users. The thresholder value is set at P, therefore, the power level of optical signals due to all classes are equal or greater than the threshold value, hence all users belonging to all M classes may cause interference on the desired user in class 1. This gives us the probability of error in a conventional one-level OCDMA system with N interfering users. In Appendix A, we obtain the BER of a conventional OCDMA system with generalized OOC. Therefore, the BER of a class 1 user with an AND logic gate structure can easily be written as follows:

$$P_{e1} = 1 + \sum_{k=1}^{w} (-1)^k \binom{w}{k} \times \left[1 + \sum_{l=1}^{\lambda} \sum_{i=l}^{\lambda} (-1)^l \binom{k}{l} \binom{w-l}{i-l} p_i\right]^N. \tag{8}$$

Now we assume that the desired user is a class 2 user. The threshold value is set at $2P$. Therefore, there are two kinds of interference: 1) the interference caused by the lower class users, i.e., class 1; 2) other users belonging to class $2, 3, \ldots, M$. Since the threshold value is set at $2P$, at least two class 1 users with power level P need to hit on a marked chip simultaneously in order to make an interference on this chip. However, other classes' users interfere normally on the class 2 users. This scenario is the same as the model studied in [3]. There are $\sum_{i=2}^{M} N_i = N - N_1$ users in the same interfering class and N_1 users in other interfering classes with a two stages interference cancellation. In general, for users in class j, we have $\sum_{i=j}^{M} N_i$ users in the same interfering class and $N_{j-1} + N_{\text{eff}_{j-1}}$ in other classes, where $N_{\text{eff}_{j-1}}$ is obtained from (3). For such a case, we obtain the BER due to class j users as $h(\sum_{i=j}^{M} N_i, N_{j-1} + N_{\text{eff}_{j-1}})$ in Appendix B.

B. ADC Structure With AND Logic Gate

We assume that the transmitted bit is "1" and the contributed interference on the kth marked chip of the desired user is α_k. An error occurs if all the first w marked chips are interfered and at least w out of $2w$ marked chips is interfered by type I interference. Now we can write the error probability as follows:

$$P_{e_j} = \Pr\big[(\alpha_1 > 0, \ldots, \alpha_w > 0 | n_j + n'_j \text{ interfering users}) \text{ and } (\text{at least } w \text{ type I hit by } n_j \text{ interfering users})\big] \tag{9}$$

where n_j and n'_j are obtained by (5) and (6), respectively. The error probability can be written as follows:

$$\begin{aligned} P_{e_j} &= \Pr(\alpha_1 > 0, \ldots, \alpha_w > 0 | n_j) + w\,[\Pr(\alpha_1 > 0, \ldots, \\ &\quad \alpha_{w-1} > 0, \alpha_w = 0 | n_j) \text{ and } (\alpha_w > 0 | n'_j)] \\ &\quad + \binom{w}{2} \Pr[(\alpha_1 > 0, \ldots, \alpha_{w-2} > 0, \alpha_{w-1} = 0, \alpha_w = 0 | n_j) \\ &\quad \text{and } (\alpha_{w-1} > 0, \alpha_w > 0 | n'_j) \text{ and } (\text{at least 2 chips} \\ &\quad \text{of } (\alpha_{w+1}, \ldots, \alpha_{2w}) > 0 | n_j)] + \cdots \end{aligned} \tag{10}$$

We can rewrite the aforementioned equation as follows:

$$P_{e_j} = \sum_{i=0}^{w} \binom{w}{i} U_i \tag{11}$$

where

$$\begin{aligned} U_i &= \Pr[(\alpha_1 > 0, \ldots, \alpha_{w-i} > 0, \alpha_{w-i+1} = 0, \ldots, \alpha_w = 0 | n_j) \\ &\quad \text{and } (\alpha_{w-i+1} > 0, \ldots, \alpha_w > 0 | n'_j) \text{ and} \\ &\quad (\text{at least } i \text{ chips of } (\alpha_{w+1}, \ldots, \alpha_{2w}) > 0 | n_j)]. \end{aligned} \tag{12}$$

U_i can be considered as the multiplication of two independent probabilities

$$U_i = Q_i \times Q_i' \tag{13}$$

where

$$Q_i = \Pr[(\alpha_1 > 0, \ldots, \alpha_{w-i} > 0, \alpha_{w-i+1} = 0, \ldots, \alpha_w = 0 | n_j) \text{ and } (\text{at least } i \text{ chips of } (\alpha_{w+1}, \ldots, \alpha_{2w}) > 0 | n_j)] \tag{14}$$

and

$$Q_i' = \Pr\left(\alpha_{w-i+1} > 0, \ldots, \alpha_w > 0 | n_j'\right) \triangleq f_{n_j'}(i). \tag{15}$$

In Appendix C, we obtain $f_{n_j'}(i)$ as a function of n_j' and i. We can write (14) as follows:

$$Q_i = \sum_{l=0}^{w-i} \binom{w}{i+l} H(l) \tag{16}$$

where we define $H(l)$ as follows:

$$\begin{aligned} H(l) &= \Pr\left[(\alpha_1 > 0, \ldots, \alpha_{w-i} > 0, \alpha_{w-i+1} = 0, \ldots, \alpha_w = 0, \right. \\ &\quad \left. \alpha_{w+1} > 0, \ldots, \alpha_{w+i+l} > 0, \alpha_{w+i+l+1} = 0, \ldots, \alpha_{2w} = 0 |\ n_j)\right] \\ &= \sum_{k=0}^{w-l} (-1)^k \binom{w-l}{k} \Pr\left(\alpha_1 > 0, \ldots, \alpha_{w+l+k} > 0 | n_j\right) \\ &= \sum_{k=0}^{w-l} (-1)^k \binom{w-l}{k} f_{n_j}(w+l+k). \end{aligned} \tag{17}$$

Using (11)–(17) we obtain

$$P_{e_j} = \sum_{i=0}^{w} \binom{w}{i} f_{n_j'}(i) \sum_{l=0}^{w-i} \binom{w}{i+l} \times \sum_{k=0}^{w-l} (-1)^k \binom{w-l}{k} f_{n_j}(w+l+k). \tag{18}$$

VI. Simulation, Analytical Results, and Discussions

In this section, we obtain the performance of the system for the two aforementioned receiver structures and compare their performance with that of the traditional one-level system. For the numerical results, we consider a multilevel system with four classes, i.e., four power levels or $M = 4$. We assume OOC codes with length $L = 100$, $\lambda = 2$, and $w = 8$. Except the desired user, we consider equal number of users for all the classes, i.e., $N_1 = N_2 = \cdots = N_M$ and $N = \sum_{i=1}^{M} N_i$. For the receiver structure without ADC, we use (B1) to obtain the error probability versus the number of users. We have shown the results in Fig. 8 along with the one-level system result. One can observe that in this case, the error probability due to class 1 users is same as that of one-level system. The reason is that the threshold value for class 1 does not reject the power level of other classes, and consequently, all users from all other classes can be considered as the interfering users such as the one-level systems. On the other hand, the performance of class 2 and class 3 are improved in relation with one-level system, while the improvement observed in the performance of class 4 users is considerable.

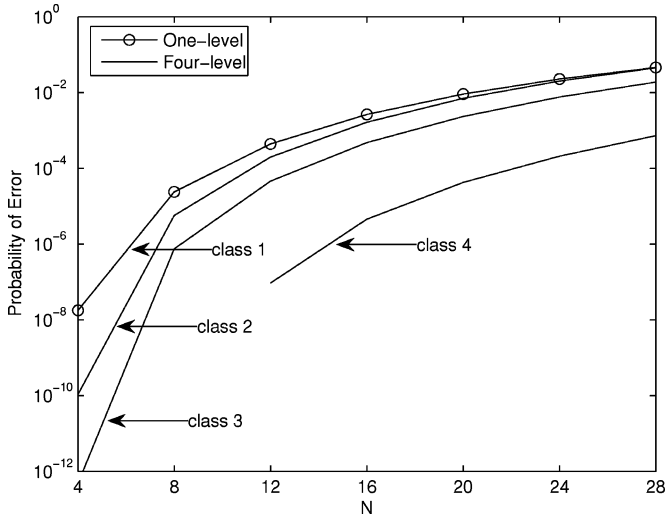


Fig. 8. Performance of one-level and four-level system with optical AND logic gate structure without ADC.

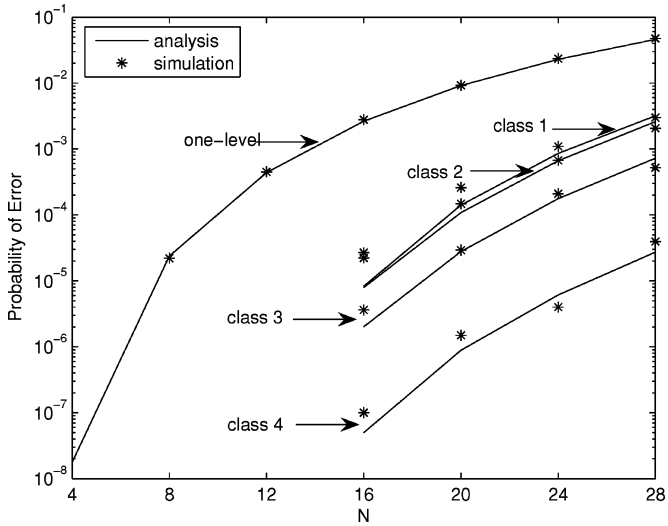


Fig. 9. Performance of one-level and four-level system with optical ADC structure with AND logic gate.

Fig. 9 shows the error probability, analytical, and simulation results, based on the receiver structure with ADC. We observe a considerable improvement in the performance as compared to one-level systems and also the receiver structure without ADC. The performance of class 1 and class 2 users do not differ so much, however the improvement of class 4 users is considerable. One can see from the figure that when the number of interfering users is less than 16 the MAI is canceled. When we have an OOC code with weight w, crosscorrelation coefficient λ and number of users $N + 1$, if $N \times \lambda < w$, then we have no MAI, since each interfering user may cause interference on λ marked chips of the desired user in the worst case. In the proposed multiclass system for class 1 if we have $N_1 < 4$, then with the selected code parameters, i.e., $w = 8$ and $\lambda = 2$, the aforementioned condition is satisfied for the users in class 1. Since other users

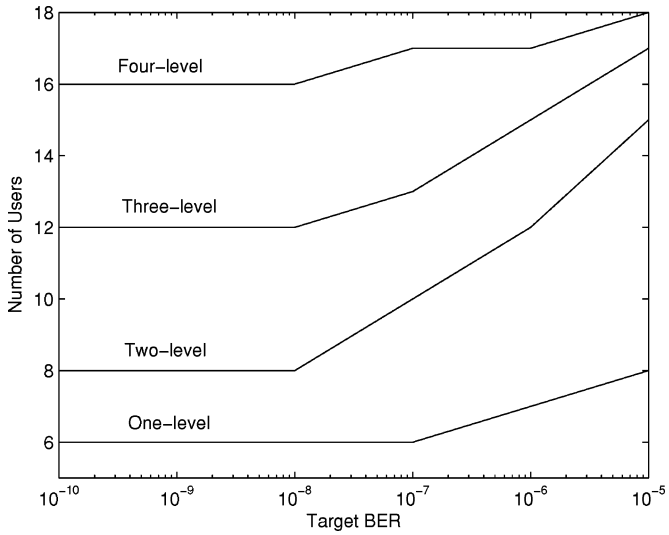


Fig. 10. Maximum allowable number of users for one-level and multilevel systems.

from the higher classes cannot make interference on the class 1 users with ADC structure, then the MAI is fully canceled. This condition can be checked for other classes considering the interference probability from higher and lower classes.

Different classes are granted different QoS by the means of error probability when the users are distributed uniformly in all classes as we observed in the results. There is another method in investigating the performance of the proposed multilevel system. We may consider that all users are distributed in M classes in such a way that the error probability belonging to all classes does not exceed a target BER. Evidently in this case, the distribution of users in different classes is not uniform and one can easily check that the number of users belonging to higher classes is more than the number of users in the lower classes. For this method, we only consider the structure with ADC, we obtain the results for the cases $M = 2$, $M = 3$, and $M = 4$, and compare their performance to the one-level system. In Fig. 10, we have obtained the maximum allowable number of users for different values of M versus the target BER. Some parameters are the same as previous figures, e.g., code parameters are $L = 100$ and $\lambda = 2$. However, we obtain the optimum value of the code weight $w = w_{\rm opt}$, according to the number of users and the Johnson bound [6]. The allowable number of users increases proportionally to the increase of number of classes as observed from Fig. 10.

VII. Conclusion

A novel multilevel multiclass OCDMA system based on all-optical processing is proposed in this paper. We suggest to distribute the users of an OCDMA network in M classes. An OOC code set with general crosscorrelation coefficient ($\lambda \geq 1$) is used as the signature sequence. We introduced a new transmitter structure in which if the power level of optical pulses due to class 1 users is equal to P, then the power level of optical pulses according to class j be equal to $2^{j-1}P$. We proposed the proper structure to construct the desired transmitter. At the receiver end, we study the well-known AND logic gate structure and we obtain its performance for the proposed system. Also we introduce a new receiver structure based on optical ADC and AND logic gate structure. We show that this receiver structure improves the system performance considerably, using the properties of optical ADC to reject the power level of opposite classes, and hence, mitigating the MAI. We obtain the system performance in two cases, 1) users are distributed uniformly in M classes, but the error probability is not symmetric; and 2) users are distributed not uniformly in M classes, but the error probability of different classes are the same. For the first case, the results BER versus number of users, show a great improvement in the system performance especially in the region that MAI is perfectly canceled. However, results of the second case indicates that the capacity of the network increases proportionally to the number of power levels or number of classes when the error probability due to each user does not exceed a predefined BER target.

Appendix A

In this appendix, we obtain the error probability due to the conventional one-level BPPM OCDMA system with generalized OOC. We denote by L, λ, w, and N, the code length, code weight, cross-correlation coefficient, and the number of interfering users, respectively. The probability of error caused by MAI is obtained as follows:

$$P_e = \frac{1}{2}\Pr\left(\text{error}|1\right) + \frac{1}{2}\Pr\left(\text{error}|0\right).$$

For a BPPM system, the two probabilities on the right hand side of the aforementioned equation are the same. Therefore, considering only the MAI effect and if we show the number of interference on the ith marked chip of the desired OOC by α_i the probability of error is obtained as follows [9]:

$$\begin{aligned} P_e &= \Pr\left(\text{error}|1\right) = \Pr\left(\alpha_1 > 0, \alpha_2 > 0, \ldots, \alpha_w > 0\right) \\ &= 1 + \sum_{k=1}^{w} (-1)^k \binom{w}{k} \Pr\left(\alpha_1 = \alpha_2 = \cdots = \alpha_k = 0\right). \end{aligned} \quad \text{(A1)}$$

We denote by $p_1, p_2, \ldots,$ and p_λ, λ probabilities with definition as p_i is the probability that one interfering user hits on exactly i specified chip pulse positions of the desired user's OOC. In an OOK and BPPM OCDMA system, the following relation is valid for the interference probabilities [9]:

$$\sum_{k=1}^{\lambda} k \binom{w}{k} p_k = \frac{w^2}{2L}. \quad \text{(A2)}$$

With the aforementioned definition, the λ events that are related to $p_1, p_2, \ldots,$ and p_λ are disjoint. Furthermore, all N interfering users are independent, and hence, we can write as follows:

$$\Pr\left(\alpha_1 = \alpha_2 = \cdots = \alpha_k = 0\right) = \left[1 + \sum_{l=1}^{\lambda} (-1)^l \binom{k}{l} \rho_l\right]^N \quad \text{(A3)}$$

where we have defined

$$\rho_l = \Pr\left(\alpha_1 = \cdots = \alpha_l = 1 | \text{ one interfering user}\right)$$
$$= p_l + \binom{w-l}{1} p_{l+1} + \cdots + \binom{w-l}{\lambda - l} p_\lambda = \sum_{i=l}^{\lambda} \binom{w-l}{i-l} p_i. \tag{A4}$$

Substituting (A4) in (A3) and using (A2), we can rewrite (A1) as follows:

$$P_e = 1 + \sum_{k=1}^{w} (-1)^k \binom{w}{k} \times \left[1 + \sum_{l=1}^{\lambda} \sum_{i=l}^{\lambda} (-1)^l \binom{k}{l} \binom{w-l}{i-l} p_i\right]^N. \tag{A5}$$

Appendix B

In this appendix, we obtain the error probability expressions due to the multilevel OCDMA system with AND logic gate receiver structure. The model we consider in this paper follows the multilevel signaling with two stage of interference canceling noted in [3]. We consider there are N_s users in the same interfering class and N_o users in the different interfering class. In this case, the probability of error is as follows:

$$h(N_s, N_o) = \sum_{i=0}^{w} \binom{w}{i} \times \left\{\sum_{m=0}^{w-i} (-1)^m \binom{w-i}{m} \left[1 + \sum_{l=1}^{\lambda} (-1)^l \binom{i+m}{l} \rho_l\right]^{N_s}\right\} \times \left\{1 + \sum_{k=1}^{2i} (-1)^k \binom{2i}{k} \left[1 + \sum_{l=1}^{\lambda} (-1)^l \binom{k}{l} \rho'_l(i)\right]^{N_o}\right\} \tag{B1}$$

where ρ_l is obtained from (A.4) and $\rho'_l(i)$ is as follows:

$$\rho'_l(i) = \sum_{j=l}^{\lambda} \binom{w-l}{j-l} p'_j(w, w') \tag{B2}$$

where $p'_j(w, w')$ is the probability that a code with weight w hit j specified chips of a code with weight w' in the case that the maximum cross-correlation value is λ, so we have

$$\sum_{k=1}^{\lambda} k \binom{w'}{k} p'_k(w, w') = \frac{w'w}{2L}. \tag{B3}$$

For a two-stage receiver structure $w' = 2i$.

Appendix C

In this appendix, we derive $f_n(i) \triangleq \Pr(\alpha_1 > 0, \ldots, \alpha_i > 0 | n \text{ interfering users})$. Each interfering user may cause interference at λ marked chips; therefore, it is evident that if $n \times \lambda < i$, then $f_n(i) = 0$. On the other hand, if $n \times \lambda \geq i$ we have

$$f_n(i) = 1 - i \times \Pr(\alpha_1 = 0) + \binom{i}{2} \times \Pr(\alpha_1 = 0, \alpha_2 = 0) - \cdots = 1 + \sum_{k=1}^{i} (-1)^k \binom{i}{k} \Pr(\alpha_1 = 0, \ldots, \alpha_k = 0) \tag{C1}$$

using (A3) we obtain

$$f_n(i) = 1 + \sum_{k=1}^{i} (-1)^k \binom{i}{k} \left[1 + \sum_{l=1}^{\lambda} (-1)^l \binom{k}{l} \rho_l\right]^n \quad n \times \lambda \geq i$$
$$f_n(i) = 0 \quad n \times \lambda < i. \tag{C2}$$

References

[1] J. A. Salehi, "Emerging OCDMA communication systems and data networks [Invited]," *J. Opt. Netw.*, vol. 6, no. 9, pp. 1138–1178, Sep. 2007.

[2] J. Ratnam, "Optical CDMA in broadband communication-scope and applications," *J. Opt. Commun.*, vol. 23, pp. 11–21, 2002.

[3] B. M. Ghaffari and J. A. Salehi, "Multiclass, multistage, and multilevel fiber-optic CDMA signaling techniques based on advanced binary optical logic gate elements," *IEEE Trans. Commun.*, vol. 57, no. 5, pp. 1424–1432, May 2009.

[4] H. Yashima and T. Kobayashi, "Optical CDMA with time hopping and power control for multirate networks," *J. Lightw. Technol.*, vol. 21, no. 3, pp. 695–702, Mar. 2003.

[5] T. Miyazawa and I. Sasase, "Enhancement of tolerance to MAIs by the synergistic effect between M-ary PAM and the chip-level receiver for optical CDMA systems," *J. Lightw. Technol.*, vol. 24, no. 2, pp. 658–666, Feb. 2006.

[6] J. A. Salehi, "Code division multiple-access techniques in optical fiber networks. Part I: Fundamental principles," *IEEE Trans. Commun.*, vol. 37, no. 8, pp. 824–833, Aug. 1989.

[7] J. A. Salehi and C. A. Brackett, "Code division multiple-access techniques in optical fiber networks. Part II: System performance analysis," *IEEE Trans. Commun.*, vol. 37, no. 8, pp. 834–842, Aug. 1989.

[8] H. M. H. Shalaby, "Chip level detection in optical code division multiple access," *J. Lightw. Technol.*, vol. 16, no. 6, pp. 1077–1087, Jun. 1998.

[9] S. Mashhadi and J. A. Salehi, "Code division multiple-access techniques in optical fiber networks. Part III: Optical AND gate receiver structure with generalized optical orthogonal codes," *IEEE Trans. Commun.*, vol. 45, no. 8, pp. 1457–1468, Aug. 2006.

[10] H. F. Taylor, "Optical analog-to-digital converter – design and analysis," *IEEE J. Quantum Electron.*, vol. 15, no. 4, pp. 210–216, Apr. 1979.

[11] A. Sawchuk and T. C. Strand, "Digital optical computing," *Proc. IEEE*, vol. 72, no. 7, pp. 758–779, Jul. 1984.

[12] B. Jalali and Y. M. Xie, "Optical folding-flash analog-to-digital converter with analog encoding," *Opt. Lett.*, vol. 20, pp. 1901–1903, 1995.

[13] L. Brzozowski and E. H. Sargent, "All-optical analog-to-digital converters, hard limiters and logic gates," *J. Lightw. Technol.*, vol. 19, no. 1, pp. 114–119, Jan. 2001.

[14] Y. Park, C. Lim, and I. Jung, "ONU power equalization of ethernet PON systems," *IEEE Photon. Technol. Lett.*, vol. 16, no. 8, pp. 1984–1986, Aug. 2004.

[15] D. Verhulst, J. Bauwelinck, Y. Martens, X.-Z. Qiu, and J. Vandewege, "A fast and intelligent automatic power control for a GPON burst-mode optical transmitter," *IEEE Photon. Technol. Lett.*, vol. 17, no. 11, pp. 2439–2441, Nov. 2005.

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