Silicon Filled Integrated Waveguides

G. Gentile, Ronald Dekker, Pascal de Graaf, M. Spirito, M. J. Pelk, L. C. N. de Vreede, and B. Rejaei Salmassi

***Abstract*—In this letter, we report, for the first time, a silicon-filled integrated waveguide based on a two mask integrated circuit (IC) process and substrate transfer technique. The fabrication process offers a high degree of control and repeatability on the device geometrical dimensions. Waveguide structures with cutoff frequencies of 35, 50, and 77 GHz were designed and fabricated. In the fundamental TE_{10}–like operating mode, average losses as low as 0.10 dB/mm with a slow-wave factor of 2.5 were observed. The measurement results are in excellent agreement with HFSS simulations, validating the usability of these structures as a new component in mm-wave IC-designs.**

***Index Terms*—Millimeter-wave, silicon filled, silicon-on-glass, substrate integrated waveguide (SIW), substrate transfer.**

TABLE I
DESIGN PARAMETERS OF THE FABRICATED STRUCTURES

Mono-modal frequency band [GHz]	35 [1]- 70 [2]	50 [1]-100 [2]	77[1]-110 [3]
Top width w_t [um]	1040	670	360
Bottom width w_b [um]	1440	1070	760
Substrate height [um]	300	300	300
Average loss [db/mm]	0.10 [4]	0.10 [5]	0.20 [6]
Average loss per wavelength [dB/ λg]	0.04 [4]	0.06 [5]	0.15 [6]
Slow wave factor	2.5 [4]	2.6 [5]	2.2 [6]

[1] Cut off of the fundamental mode (TE_{10}-like); [2] cut off of the first higher order mode.

[3] Maximum measured frequency. The simulated cut-off of the first higher order mode is 123 GHz.

[4] at 50 GHz; [5] at 75 GHz; [6] at 100 GHz..

I. INTRODUCTION

MODERN monolithic microwave integrated circuits (MMIC's) make commonly use of planar transmission lines to transfer and process high-frequency signals. Despite their ease of fabrication, however, integrated transmission lines are prone to high losses. At millimeter wave frequencies (e.g., above 30 GHz), conductor loss alone can easily exceed several dB/cm [1]. Moreover, depending on the substrate permittivity and thickness [2], substrate surface waves may be excited leading to additional attenuation and crosstalk effects.

These limitations have motivated the recent investigation of substrate-integrated waveguides (SIW) as an alternative [3], [4]. The vertical sidewalls of these structures consist of arrays of closely-spaced metallic via holes embedded in the underlying dielectric substrate, whereas their horizontal surfaces are formed by conventional patterning of metal layers on the top and bottom of the substrate. SIW's are superior to transmission lines in terms of conductor loss and provide a significantly lower crosstalk due to the higher field confinement.

Nevertheless, the application of SIW's has so far been limited to traditional microwave substrates (e.g., high frequency laminate, LTCC and HTCC) [3]–[5] where vertical via holes are simply 'punched' through the wafer using conventional workshop techniques. Such methods bring about severe limitations in terms of reproducibility and minimum feature size resolution when targeting mm-wave components. These limitations can only be overcome by developing a process based on IC photo-lithography technology, as was proposed in [5], [6].

In this letter we present an IC compatible process, based on substrate transfer technology [7], [8] which allows the integration of waveguides with continuous metallic sidewalls in a silicon substrate. The result is a cavity waveguide filled with high-resistivity (e.g., 0.7–1.3 $\mathrm{k}\Omega \cdot \mathrm{cm}$) silicon. Feeding structures (e.g., coplanar to waveguide transitions) have also been implemented to connect the waveguide to the planar structures present on the IC. Waveguide structures with different cutoff frequencies (e.g., 35, 50 and 75 GHz) are designed and implemented. The measured results exhibit average losses as low as 0.10 dB/mm or 0.04 db/guideded wavelength (see Table I for results summary). Furthermore, the relatively high dielectric constant of silicon leads to a typical 2.5 fold reduction of propagation wavelength which is an important advantage of these structures given the stringent requirements imposed on device size in modern IC technology.

II. FABRICATION

In conventional IC technology the substrate (e.g., silicon) provides the dielectric material for device integration and, at the same time, acts as a mechanical carrier giving stability to the circuit. By contrast, substrate transfer technology [7], [8] separates the two roles: devices can still be implemented on silicon, while a different substrate such as glass is employed as the mechanical carrier. This allows the 3-D structuring of the silicon substrate using IC compatible processes, such as in the silicon-filled waveguides described below.

The process begins with a high resistivity (e.g., 0.7–1.3 $\mathrm{k}\Omega \cdot \mathrm{cm}$) $\langle 100 \rangle$ oriented silicon wafer which is grinded back until the desired height (e.g., 310 μm), followed by 10 μm wet damage etch. Next, 50 nm of low-stress LPCVD nitride is deposited, and

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G. Gentile, M. Spirito, M. J. Pelk, L. C. N. de Vreede, and B. Rejaei Salmassi are with the DIMES Institute, Delft University of Technology, Delft 2628 CT, The Netherlands (e-mail: g.gentile@tudelft.nl; m.spirito@tudelft.nl; M.J.Pelk@tudelft.nl; l.c.n.devreede@tudelft.nl; b.rejaei@ewi.tudelft.nl).

R. Dekker is with the Philips Research Laboratories, Eindhoven 5656 AA, The Netherlands. He is also with the DIMES Institute, Delft University of Technology, Delft 2628 CT, The Netherlands (e-mail: ronald.dekker@philips.com).

P. de Graaf is with the Philips Research Laboratories, Eindhoven 5656 AA, The Netherlands (e-mail: pascal.de.graaf@philips.com).

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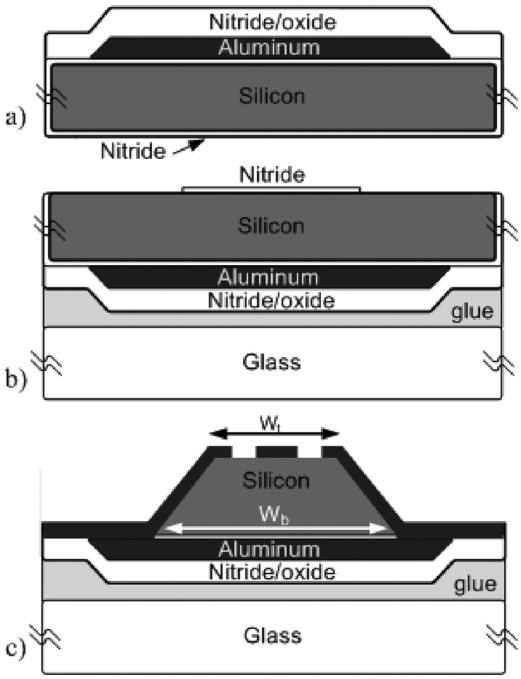

Fig. 1. Technology steps. After aluminum deposition (a), the silicon wafer is glued top down to a glass carrier (b), and waveguide sidewalls are defined via KOH etching (c).

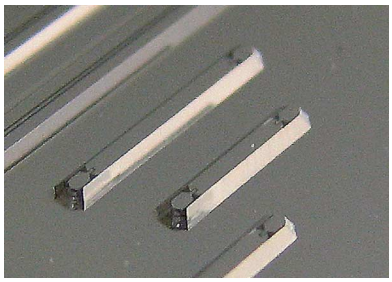

Fig. 2. Waveguides camera made picture. Metal layers are in dark grey, sidewalls in light grey, and transition slots in black.

1 μm of Al is sputtered on the front side of the wafer. Then, the aluminum is removed from the edge of the wafer and two layers of respectively 0.5 μm PECVD nitride and 0.5 μm PECVD oxide are deposited [see Fig. 1(a)]. The silicon wafer is glued, top down, to a glass carrier, which provides the required mechanical support for the next steps.

Next, the nitride is patterned on the exposed side of the wafer [see Fig. 1(b)] and the silicon is etched using a KOH solution [7], [8]. Since KOH etching is anisotropic, a trapezoidal cross section is created. Next a 1 μm-thick layer of Al is sputtered to implement the top horizontal wall and the waveguide side walls. To complete the process, the top aluminum layer is patterned by using resist spray coating, followed by contact lithography and wet chemical etching [see Fig. 1(c)]. Fig. 2 shows a picture of the final structure. Note that during the etch process, undercutting at convex corners occurs; for this reason extra features called corner compensation structures are added [9].

III. Design

Conventional rectangular waveguides employ TE_{10} as the fundamental mode of operation. To dimension the structure simple equations (e.g., width to height ratio of 2) ensure that only the fundamental mode propagates in a broad frequency range with minimum losses. HFSS simulated field distribution of a waveguide with trapezoidal cross-section strongly resembles that of a rectangular one of width $\mathrm{w_{avg}} = (\mathrm{w_t} + \mathrm{w_b})//2$, where $\mathrm{w_t}$ and $\mathrm{w_b}$ represent the width of the top and bottom horizontal walls, respectively [Fig. 1(c)]. Therefore, we can assume that a TE_{10}–like mode is the fundamental propagating mode in the structures presented in this letter.

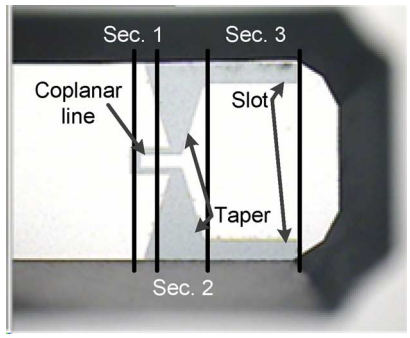

Fig. 3. Optical microscope photo of coplanar-to-waveguide transition. Waveguide sidewalls are in black (off-focus), and the top metallization in white, on which the slot transition can be seen in light grey.

The design parameters of the implemented structures are summarized in Table I. Multiple waveguide lengths for each geometry were implemented (e.g., 1, 2, and 4 cm) in order to remove the effect of the transition using a de-embedding algorithm [10]. Note that since all the waveguides are implemented on the same substrate, their height is constant (300 μm) and cannot be scaled to half of the width if different cutoff frequencies are to be realized. This leads to a slight increase in loss of the lower cutoff geometries (e.g., 35 and 50 GHz).

To feed and probe the waveguide, transition structures were designed which couple the TEM mode of a coplanar waveguide transmission line (CPW) to the TE_{10}–like mode of the waveguide. The transition is composed of three sections (see Fig. 3): a coplanar line, a tapered slot antenna, and two loading resonating slots. The transition starts with a 50 Ω CPW line realized on the top metal layer where high frequency measurement probes can be easily landed. After this section, a half-wavelength tapered slot antenna is implemented in order to match the electric field distribution of the resonating slot mode to the TE_{10} waveguide mode. Since slot-based CPW to waveguide transitions provide a narrow matching bandwidth with a half wavelength antenna [11], two quarter-wavelength slot loads (along the guide) were used to terminate the half-wavelength tapered slot. This gives a total slot length of one wavelength which ensures a broader impedance bandwidth [12].

IV. Measurement and Results

The waveguides were characterized by means of their S-parameters measured by an Agilent E8361C PNA with mm-wave module extensions to cover the 65–110 GHz band. The high frequency signal was delivered to the integrated structures using Cascade Microtech 110 GHz Infinity probes.

Fig. 4 shows the performance of a waveguide with the implemented transitions. The relatively poor matching observed can be explained by KOH process inaccuracy, resulting in an under etch of straight lines and convex corners which reduced

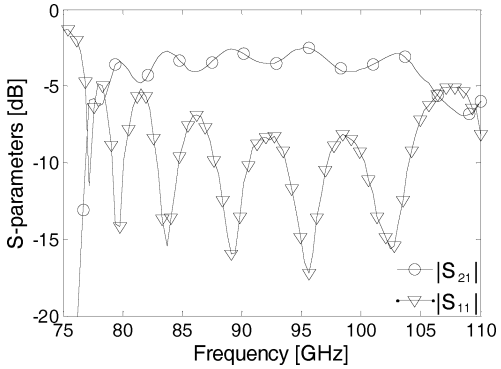

Fig. 4. S-parameters of 2.5 mm waveguide with transitions.

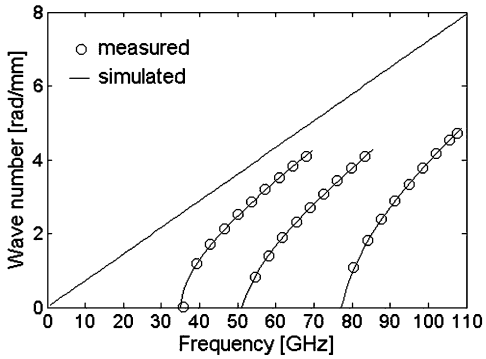

Fig. 5. Dispersion diagram: simulations versus measurements comparison. The straight line corresponds to the case of a TEM mode in silicon.

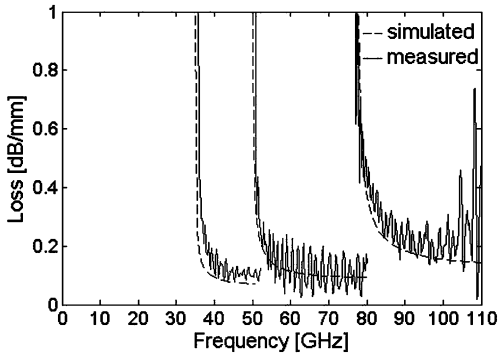

Fig. 6. Waveguide losses: simulations versus measurements comparison. Losses are expressed as $10 \cdot \log_{10} \exp(-2 \cdot \alpha \cdot \mathrm{d}))$ choosing $\mathrm{d} = 1\ \mathrm{mm}$.

transition geometrical dimensions. To remove the transition effects and extract the parameters of the line, we employed a L-2L de-embedding method [10].

Fig. 5 shows the simulated and measured dispersion diagrams for integrated waveguides with various cutoff frequencies after de-embedding. The simulations were performed using Ansoft HFSS where a silicon bulk resistivity of $715\ \Omega \cdot \mathrm{cm}$ was assumed. The three measured curves strongly resemble the well-known bulk waveguide behavior: no propagation below the cutoff, strongly dispersive just above cutoff, and linear well above it. Comparing to an air-filled waveguide, the obtained slow-wave factors are reported in Table I.

Fig. 6 shows the attenuation constant in dB per mm, for the three structures. Well beyond the cutoff, in the single-mode propagation range, losses are almost constant versus frequency and match the simulated values. Average insertion losses of 0.10, 0.10 and 0.20 dB/mm were measured for the 35, 50, and 77 GHz cutoff structures, respectively (see Table I).

V. Conclusion

Integrated waveguides using silicon as dielectric filling material have been fabricated using substrate transfer technique. Compared with traditional integrated transmission lines, these waveguides exhibit very low average losses (0.1–0.2 dB/mm). Moreover, the silicon filling yields a slow-wave factor of 2.5 compared to air-filled devices, which facilitates the integration of compact waveguide devices.

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References

[1] T. S. D. Cheung, J. R. Long, K. Vaed, R. Volant, A. Chinthakindi, C. M. Schnabel, J. Florkey, and K. Stein, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, Feb. 2003, pp. 396–397.

[2] R. W. Jackson, "Mode conversion at discontinuities in finite-width conductor-backed coplanar waveguide," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-37, no. 10, pp. 1582–1589, Oct. 1989.

[3] D. Deslandes and K. Wu, "Single-substrate integration techniques of planar circuits and waveguide filters," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 2, pp. 593–596, Feb. 2003.

[4] K. Wu, "The substrate integrated circuits – A new concept for high-frequency electronics and optoelectronics," in *Proc. IEEE 6th Conf. Telecommun. Modern Satellite, Cable Broadcasting Service (TELSIKS'03)*, Oct. 2003, vol. 1, pp. P-III–P-X.

[5] W. R. McGrath, C. Walker, M. Yap, and Y.-C. Tai, "Silicon micromachined waveguides for millimeter-wave and submillimeter-wave frequencies," *IEEE Microw. Guided Lett.*, vol. 3, no. 3, pp. 61–63, Mar. 1993.

[6] M. Henry, C. E. Free, B. S. Izqueirdo, J. Batchelor, and P. Young, "Millimeter wave substrate integrated waveguide antennas: Design and fabrication analysis," *IEEE Trans Adv Packag.*, vol. 32, no. 1, pp. 93–99, Feb. 2009.

[7] R. Dekker, P. G. M. Baltus, and H. G. R. Maas, "Substrate transfer for RF technologies," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 747–757, Mar. 2003.

[8] K. Buisman, L. K. Nanver, T. L. M. Scholtes, H. Schellevis, and L. C. N. de Vreede, "High-performance varactor diodes integrated in a silicon-on-glass technology," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2005, pp. 117–120.

[9] P. Pal, K. Sato, and S. Chandra, "Fabrication techniques of convex corners in a (1 0 0)-silicon wafer using bulk micromachining: A review," *J. Micromech. Microeng.*, pp. 17:R111–R133, Oct. 2007.

[10] Y. Tretiakov, J. Rascoe, K. Vaed, W. Woods, S. Venkatadri, and T. Zwick, "A new on-wafer de-embedding technique for on-chip RF transmission line interconnect characterization," in *Proc. ARFTG Conf. Dig.*, Jun. 2004, pp. 69–72.

[11] D. Deslandes and K. Wu, "Integrated transition of coplanar to rectangular waveguides," in *Int. Microw. Symp. Dig.*, May 2001, vol. 2, pp. 619–622.

[12] A. Patrovsky, M. Daigle, and K. Wu, "Millimeter-wave wideband transition from CPW to substrate integrated waveguide on electrically thick high-permittivity substrates," in *Proc. IEEE Microw. Conf.*, Oct. 2007, pp. 138–141.